University of Cape Town

Towards A Single Electron Current On Superfluid Helium

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ABSTRACT

The aim of this dissertation was to investigate the application of a system of electrons floating above the surface of superfluid helium to the field of single electron transport. Previous work done by Dr Forrest Bradbury at Princeton University (now a collaborator in the group) demonstrated the highly efficient and precise control of packets of electrons floating on the surface of superfluid helium, localised to channels defined in a silicon substrate.

Using similar devices and methodologies, the work done in this dissertation investigates whether this modality of electron transport can be effectively applied to deliver a current of single electrons.

Single electron devices have numerous applications in the field of metrology and quantum information processing. They allow for measurements to be made of fundamental quantities, such as the charge of an electron, and further demonstrate various quantum mechanical properties of nature.

Presented in this dissertation is the work completed to date, which includes: the design and fabrication of the nanoscale device used to conduct the electrons on superfluid helium experiments, the required electronics needed to control the device and the data acquisition system needed to read various signals off the device. The fabrication was done at Oak Ridge National Labs in the USA. Additionally, a hermetically sealed superfluid cell designed in collaboration with Dr Jay Amrit from Université Paris-Sud, France used to house the device is presented, as well the probe needed to insert this cell into the dilution fridge.

The theory behind the functionality of the device and the way in which it would work is developed. A simulation of working of the device is presented, as well as the expected measurement quantities.

The outlook for continued work in this exciting and very novel physical system is also presented.

DEDICATION

I dedicate this dissertation to my late father, Rainer Funk, who passed away 10 years ago. You will be forever missed.

Now, *ab hinc ego vade.*

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Declaration

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LIST OF ACRONYMS

SET
Single Electron Transport. 1, 2, 11

TISE
Time-Independent Schrödinger Equation. 5, 22

DOS
Density of States. 7–9

MFP
Mean Free Path. 9

CCD
Charge-Coupled Device. 23

CNMS
Centre for Nanophase Material Science. 25, 26, 82

FEM
Finitie Element Modelling. 25, 32

HEMT
High Electron Mobility Transistor. 33, 68, 70

KCL
Kirchhoff's Current Law. 35

EBL
Electron Beam Lithography. 43, 50, 54, 82

ALD
Atomic Layer Deposition. 46, 47

BHF
Buffer Hydrofluoric Acid. 47, 54

PECVD
Plasma-Enhanced Chemical Vapour Deposition. 47

RIE
Reactive Ion Etching. 47, 54

PEC
Proximity Effect Correction. 50

SEM
Scanning Electron Microscope. 50

PCBs
Printed Circuit Boards. 60, 61, 67, 71, 82, 83

MBD
Motherboard. 60

DHB
Device Holding Board. 60

LIST OF CONSTANTS

$\hbar$ $1.05 \times 10^{-34}\,\mathrm{J\,s}$
The reduced Planck constant. 5, 7–9, 22

$\mathrm{m_e}$ $9.10 \times 10^{-31}\mathrm{kg}$
The electron (rest) mass. 5, 22, 23

$\mathrm{k_B}$ $8.62 \times 10^{-5}\mathrm{eV/K}$
The Boltzmann constant. 6, 38

e $1.60 \times 10^{-19}\mathrm{C}$
The universal constant of elementary charge. 9, 11, 19–23, 32, 33, 37, 38

ϵ_{He} $9.36 \times 10^{-12}\mathrm{F/m}$
The permittivity of liquid helium at around 1 K with $\epsilon_r = 1.0572$. 19–21, 33, 38

CHAPTER 1

INTRODUCTION

Electrons on superfluid helium present an opportunity to investigate a physical system with unique and interesting properties. Electrons become bound to the surface of the superfluid by their own image potential induced in the weakly polarizable fluid, which attracts them towards it. However, they are prevented from breaking through it due to the large energy barrier ($\sim 1\,\mathrm{eV}$) established by the Pauli exclusion principle [5]. These opposing energies create a potential environment in which the charges will, in their ground state, float approximately 100 Å above the surface, forming a two-dimensional electron gas system (2DEG) above the surface.

A 2DEG established in this manner has a very low density and is thus in a purely non-degenerate state. This is mainly caused by the strong Coulomb interactions between the charges which are largely unscreened given the very small dielectric constant of liquid helium ($\epsilon_r \simeq 1.057$). The charges in this system are also very well isolated above the fluid film and exhibit some of the highest mobilities of any system (exceeding 10^7cm/Vs [6]), due to the minimal scattering events that can occur given the properties of superfluid ^{4}He. These two distinguishing characteristics have been used to study a wide variety of different physical phenomena such as investigating the topological surface structure of superfluid ^{4}He [7], Wigner crystallisation [8], Coulomb liquids [9]) and as a way to implement a scalable quantum computing chip [10].

The high mobilities of the charges in this system could be applied to the field of Single Electron Transport (SET) to deliver an accurate single electron current that can remain coherent for a long period of time. This is the main reason for the focus of this thesis on this work. The novel application of this type of charge system to the field of SET could allow one to explore SET in a new regime, where experiments that require single electrons with high

mobilities and coherence times can be performed.

This work was inspired by the previous work done by Bradbury et al. [11] at Princeton University, who demonstrated precise and efficient control over the position of packets of charges along superfluid ^{4}He channels. The work by Papageorgiou et al. [12] demonstrated the ability to count individual electrons passing in and out of a quantum dot above superfluid films, and by Rees et al. [13] and Lin et al. [14], who implemented split gates in superfluid ^{4}He, also gave merit to the application of the system to SET.

The device designed in this thesis implements a turnstile type gate arrangement, similar to the early SET turnstile pumps of Kouwenhoven et. al. [1]. The primary functional goal of this device was to clock a predetermined amount of charge through the turnstile gates, determined by the clocking frequency and duration, and then to measure the amount of charge that was clocked through using a capacitive charge sensing technique (instead of a direct current measurement). If the measured value fell within the uncertainty limits of the expected value then we could be sure that: 1. quantised single-electron transport was indeed achieved and 2. the capacitive charge sensing measurement worked and was accurate.

One of the main challenges with using this approach is the inability to make direct contact with the 2DEG, preventing a direct current measurement of the pumped charge. A possible approach to solving this may be to use a gate that allows charges to tunnel through it if a sufficiently attractive potential is applied. This has not yet been shown and is an additional goal of this project.

In summary, the following research questions were asked to focus the scope and drive of this thesis:

- Can a controllable single electron current be achieved using the modality of electrons on superfluid ^{4}He?
  More precisely, after pumping electrons at a certain frequency for a period of time, does the total theoretical amount of transported charge Q_{theo} correspond to the amount measured using the capacitive charge sensing technique Q_{meas}?
- Can this accumulated charge be drained as a direct current? If so, does the total current measurement correspond to the amount sensed (Q_{meas} from the above)?

Because this project was entirely new to the Nanoelectronics group at UCT, the infrastructure required to conduct the necessary experiments had to be built. Guided by the above research questions, the actual work done and output of this thesis has been the design and implementation of these infrastructural requirements: the design and fabrication of the device and all the electronics needed to control and use it, the hermetically sealed cell required to house it all inside the dilution fridge, as well as the probe needed to lower the cell into the dilution fridge.

The research questions as posed above will only be answered at the conclusion of the collaborative effort to implement this system. This work done is in an effort towards establishing the foundations of this large collaborative project.

CHAPTER 2

THEORY

2.1 Review of Mesoscopic Physics

Mesoscopic physics is a sub-branch of condensed matter physics (large collections of atoms) involving the study of mesoscopic systems: materials, structures or devices with feature sizes comparable to the characteristic lengths of the objects of interest, usually electrons. The size of these systems is generally in the order of between 1 µm to 100 nm, making nanofabrication and nanotechnology closely related fields, where both classical and quantum rules may apply [15]. These systems are fabricated using various techniques such as Molecular Beam Epitaxy (MBE) [16], vapour deposition, metal evaporation, semiconductor etching and more, being experimentally realised at low temperatures in a cryostat, such as a dilution refrigerator [15].

One of the main goals of mesoscopic experiments are to investigate the electronic transport characteristics of materials [15]. These materials are commonly crystalline, semiconductor heterostructures in the solid-state. In this dissertation, however, electronic transport on top of a film of superfluid helium is investigated.

2.2 Foundational Concepts

The transport characteristics of mesoscopic devices or systems can be investigated by deriving the allowed electron energy eigenstates and eigenvalues for that system using the famous Time-Independent Schrödinger Equation (TISE)

$$\hat{\mathcal{H}}\psi(\mathbf{r}) = E\psi(\mathbf{r})\,,$$
$$\hat{\mathcal{H}} = \left[-\frac{\hbar^2}{2\mathrm{m_e}}\nabla^2 + V\right], \tag{2.1}$$

where

E is the energy of $\psi(\mathbf{r})$

$\hat{\mathcal{H}}$ is the (time-independent) Hamiltonian of the system, defined by the confining potentials V that exist within it and the Laplacian ∇^2,

$\psi(\mathbf{r})$ is the value of the wave-function of an electron at position $\mathbf{r}$ inside the system.

In this section, crystalline materials with periodic potentials are analysed and in doing so, foundational concepts that apply to many mesoscopic systems, such as the Density of States, are derived.

2.2.1 Bloch Waves

For electrons in a crystal lattice with a periodic potential $U(\mathbf{r})$, Eq. 2.1 can be rewritten as

$$\psi'' + \chi^2(E - U(\mathbf{r}))\psi = 0, \quad \chi^2 = \frac{2}{\hbar^2}, \tag{2.2}$$

(ψ still a function of $\mathbf{r}$).

Bloch's theorem states that due to the symmetric nature of the periodic potential, the translation operator commutes with the Hamiltonian $\hat{\mathcal{H}}$ of the lattice, making a Bloch wave a valid energy eigenstate and therefore a basis for solutions to Eq. 2.2, given by [16]

$$\psi_{n,\mathbf{k}}(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}}u_{n,\mathbf{k}}(\mathbf{r})\,, \tag{2.3}$$

where

$\mathbf{k}$ is the 3-component wave vector for the x, y, z-directions,

$u_{n,\mathbf{k}}(\mathbf{r})$ is a periodic function with the same periodicity as $U(\mathbf{r})$.

For each $\mathbf{k}$, there are multiple solutions to Eq. 2.2 corresponding to different energy bands within the lattice labelled by n, the band index. Together $n, \mathbf{k}$ identify a unique eigenstate. For each band, there exists an energy dispersion relation $E_n(\mathbf{k})$ that varies 'smoothly' with changes in $\mathbf{k}$.

Bloch waves exhibit the following translation property, that after a translation $\mathbf{T}$ on some Bravais lattice for a material

$$\begin{gathered}\psi(\mathbf{r}+\mathbf{T}) = e^{i\mathbf{k}\cdot(\mathbf{r}+\mathbf{T})}u_{n,\mathbf{k}}(\mathbf{r}+\mathbf{T}) = e^{i\mathbf{k}\cdot\mathbf{T}}e^{i\mathbf{k}\cdot\mathbf{r}}u_{n,\mathbf{k}}(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{T}}\psi(\mathbf{r})\,, \\ \mathbf{T} = \mathbf{N}\cdot\hat{\mathbf{a}} = N_1\boldsymbol{a}_1 + N_2\boldsymbol{a}_2 + N_3\boldsymbol{a}_3\,, \quad N_i \in \mathbb{Z}\,,\end{gathered} \tag{2.4}$$

where $\boldsymbol{a}_i$ is the primitive lattice vector, with $|\boldsymbol{a}_i|$ being the interatomic distance in the i-th crystallographic direction.

Given that the electrons are in a periodic potential (i.e. $U(\mathbf{r}) = U(\mathbf{r}+\mathbf{T})$), the Born–von Karman (BVK) periodic boundary condition

$$\psi(\mathbf{r}+\mathbf{T}) = \psi(\mathbf{r})\,, \tag{2.5}$$

can be used, which restricts the wave-function to being periodic after a translation by $\mathbf{T}$ for some large $\mathbf{N}$. This is useful in understanding what happens during quantum confinement (see Sec. 2.2.4) as $\mathbf{N}$ becomes small in one or more dimensions.

Combining the translation property of Bloch waves and the BVK boundary conditions to give

$$e^{i\mathbf{k}\cdot\mathbf{T}} = 1\,, \tag{2.6}$$

the allowed values of $\mathbf{k}$ can be derived.

For a cubic lattice [15]

$$k_x = \frac{2\pi}{L_x}n_x, \quad k_y = \frac{2\pi}{L_y}n_y, \quad k_z = \frac{2\pi}{L_z}n_z, \quad n_i \in \mathbb{Z}\,, \tag{2.7}$$

where $L_i = N_i|\boldsymbol{a}_i|$ is the total length in the i-th crystallographic direction.

2.2.2 Fermi Level and Fermi Energy

The Fermi-Dirac distribution function gives the probably that, for a system in thermal equilibrium at a temperature T, a state with energy E is occupied:

$$f(E,T) = \frac{1}{e^{\frac{E-E_f}{k_B T}}+1}\,. \tag{2.8}$$

For $T > 0\,\mathrm{K}$, E_f is defined as the *Fermi level*, the energy at which the probability of occupancy is 0.5. However, as $T \to 0\,\mathrm{K}$, Eq. 2.8 becomes a step function and E_f is defined as the *Fermi energy*, the energy of the highest occupied state at 0 K [15]. The distinction is important, as the Fermi energy is an inherent property of a material and can be derived. The Fermi level is dependent on the temperature.

The Fermi energy determines many properties of a material depending on where it falls in the material's energy dispersion, notably whether it is a metal (or semi-metal), a semiconductor or an insulator.

2.2.3 Effective Mass

Electrons in the conduction band can, with minimal energy, change to new states since the conduction band has many unoccupied states within it. This underpins conduction in materials and can be approximated well for an isotropic material using a second-order Taylor series expansion of its dispersion relation at the valence band minima E_c, as it is smooth with zero first derivative [16]:

$$\begin{aligned} E(\mathbf{k}) &= E_c + \frac{1}{2}\frac{\partial^2 E}{\partial \mathbf{k}^2}|\mathbf{k}|^2 \\ &= E_c + \frac{\hbar^2}{2\mathrm{m}_\mathrm{e}^*}|\mathbf{k}|^2, \quad \mathrm{m}_\mathrm{e}^* = \frac{\hbar^2}{\partial^2 E/\partial \mathbf{k}^2}\,. \end{aligned} \tag{2.9}$$

This relation, called the parabolic band approximation, is equivalent to the dispersion relation for electrons with an *effective mass* m_e^* satisfying the TISE (Eq. 2.1) of the form:

$$\left[-\frac{\hbar^2}{2\mathrm{m}_\mathrm{e}^*}\nabla^2\right]\psi(\mathbf{r}) = E\psi(\mathbf{r})\,. \tag{2.10}$$

With no confining potential, these electrons can be modelled as quasifree, unbounded particles that ballistically travel through the lattice, undergoing only elastic scattering with nucleus ions ($|\mathbf{k}|$ does not change, only the direction).

2.2.4 Quantum Confinement and Density of States

The effect a confining potential has on a crystalline material system is most clearly and usefully demonstrated by analysing the system's Density of States (DOS) in some region, which is the number of electron states it has per unit volume, per energy and is given by

$$g_\mathcal{D}(E) = \frac{s}{V_\mathcal{D}}\frac{\mathrm{d}N_\mathcal{D}}{\mathrm{d}\mathbf{k}}\frac{\mathrm{d}\mathbf{k}}{\mathrm{d}E_\mathcal{D}}\,, \tag{2.11}$$

where

- $\mathcal{D}$ is the system's degree of freedom,
- s is the spin degeneracy for electrons ($s = 2$),
- $V_\mathcal{D}$ is the per-unit volume factor,
- $N_\mathcal{D}(\mathbf{k})$ is the number of states at or below $|\mathbf{k}|$ in the context of the *Fermi surface* that the dispersion relation makes in the reciprocal space,
- $E_\mathcal{D}(\mathbf{k})$ is the dispersion relation, with which $\mathbf{k}(E_\mathcal{D})$ can be found.

It can be shown that for isotropic materials, $V_\mathcal{D} = (2\pi)^\mathcal{D}$ and $N_\mathcal{D}(\mathbf{k})$ is

$$N_3(\mathbf{k}) = \frac{4}{3}\pi|\mathbf{k}|^3, \quad N_2(\mathbf{k}) = \pi|\mathbf{k}|^2, \quad N_1(\mathbf{k}) = 2|\mathbf{k}|. \tag{2.12}$$

The above is derived by approximating $\mathbf{k}$ as a continuous variable, which is valid only in each unbounded direction (no confining potential) due to large L_i from Eq. 2.7, and integrating $|\mathbf{k}|$ from $0 \rightarrow |\mathbf{k}_f| = \sqrt{2\mathrm{m}_\mathrm{e}^* E_f}$ (states at the Fermi energy).

If a confining potential is imposed, L_i in the direction of the confinement becomes small and the discrete, quantized nature of the component k_i dominates, meaning the integral in that direction is not defined.

Bulk, 3DEG

For the dispersion given in (Eq. 2.9), with no confining potential, the DOS for a three degree of freedom system (in the bulk of a material) is [17]

$$g_3(E) = \frac{1}{2\pi^2}\left(\frac{2\mathrm{m}_\mathrm{e}^*}{\hbar^2}\right)^{3/2}\sqrt{E - E_c}\,. \tag{2.13}$$

2DEG

For a confinement in the z-direction only, the TISE (Eq. 2.1) takes the form [17]

$$\left[-\frac{\hbar^2}{2\mathrm{m}_\mathrm{e}^*}\nabla^2 + V(z)\right]\psi(\mathbf{r}) = E\psi(\mathbf{r})\,. \tag{2.14}$$

This two degree of freedom (2DEG) system and has a dispersion relation and DOS given by

$$E_{n_z}(\mathbf{k}) = \frac{\pi^2\hbar^2}{2\mathrm{m}_\mathrm{e}^*}\left(\frac{n_z}{L_z}\right)^2 + \frac{\hbar^2}{2\mathrm{m}_\mathrm{e}^*}|\mathbf{k}|^2\,, \tag{2.15}$$

$$g_2(E) = \frac{\mathrm{m}_\mathrm{e}^*}{\pi\hbar^2}\,, \tag{2.16}$$

where $\mathbf{k}$ is now a 2-component vector in the x and y-directions. Due to the confinement in the z-axis, the dispersion is quantised in n_z.

1DEG, Quantum Wire

Similarly, for a system confined in both the y and z-directions, with only one degree of freedom (a 1DEG or a quantum wire), the dispersion and DOS are [17]

$$E_{n_y,n_z}(k_x) = \frac{\pi^2\hbar^2}{2\mathrm{m}_\mathrm{e}^*}\left[\left(\frac{n_z}{L_z}\right)^2 + \left(\frac{n_y}{L_y}\right)^2\right] + \frac{\hbar^2}{2\mathrm{m}_\mathrm{e}^*}k_x^2\,, \tag{2.17}$$

$$g_1(E) = \frac{1}{2\pi}\left(\frac{2\mathrm{m}_\mathrm{e}^*}{\hbar^2}\right)^{1/2}\frac{1}{\sqrt{E - E_c}}\,. \tag{2.18}$$

0DEG, Quantum Dot

For a total confinement, the energy is completely quantised and the DOS becomes a line spectrum, similar to that of an atom, [17]

$$E_{n_x,n_y,n_z} = \frac{\pi^2\hbar^2}{2\mathrm{m}_\mathrm{e}^*}\left[\left(\frac{n_z}{L_z}\right)^2 + \left(\frac{n_y}{L_y}\right)^2 + \left(\frac{n_x}{L_x}\right)^2\right],$$

$$g_0(E) = 2\delta(E - E_c)\,.$$

The Fermi-Dirac probability distribution of Eq. 2.8 and the DOS $g_\mathcal{D}(E)$ can be used to find the density of *occupied* states.

2.2.5 Mean Free Path and Ballistic Transport

The Mean Free Path (MFP) l_e of a system of electrons, unbounded in one or more directions, is the average distance travelled by each charge before undergoing scattering, given by [15]

$$l_e = v_f \tau_{sc}\,, \tag{2.19}$$

$$v_f = \sqrt{\frac{2E_f}{\mathrm{m}_\mathrm{e}^*}}\,, \tag{2.20}$$

where

τ_{sc} is the average scattering time,

v_f is the Fermi velocity,

E_f is the Fermi energy.

The movement of charges between distances smaller than the MFP is called ballistic transport. The mobility μ of a system is related to the MFP by $\mu = \mathrm{e}\,l_e/v_f\mathrm{m}_\mathrm{e}^*$. If $L_i < l_e$ for some quantum wire, conducting electrons would, on average, move through the wire unhindered. Although this might seem to imply an infinite conductance, remarkably the measured conductance is in fact quantised in integer multiples of $2e^2/h$, as predicted by quantum mechanics. This underpins one of the most important phenomena in mesoscopic physics, the Quantum Hall effect [15].

2.2.6 Phase Coherence Length

The phase coherence length l_ϕ of an electron is the average distance after which the original phase is randomized [15], decohering from its original state. This is caused by scattering events such as those with other electrons (electron-electron), the periodic lattice potential (electron-phonon), vacancy centres, defects and more.

During these events, an electron's energy and momentum change. A *thermalisation* process is said to occur during electron-phonon scattering events in which a system will reach thermal equilibrium due to these energy exchanges.

Phase coherence is a necessary condition for energy quantisation, meaning the length of confinement L_i must be in the order of or smaller than l_ϕ for the effect to occur. Aharonov–Bohm oscillations [18] are an interesting consequence of coherent phase interference. A single electron passing through a ring-shaped structure will spilt into two entangled pairs that recombine with a resulting phase altered by the magnitude of an applied magnetic field.

2.3 Single Electron Transport

SET is one of the key research fields in mesoscopic physics. It involves defining systems that exploit the quantum mechanical properties of materials, to move single electrons from source to drain to produce highly accurate currents of the form

$$I_{DS} = nef\,, \tag{2.21}$$

where

n is the number of electrons transported per cycle,

e is the universal elementary charge of the electron,

f is the transport frequency.

One of the main applications of SET is in the field of quantum metrology [19], which seeks to define quantities in terms of universal constants. The ampere, for example, can be defined in terms of Eq. 2.21. The volt is currently defined using the Josephson effect realised on a superconducting Josephson junction [20] and the ohm using the quantum Hall effect [20]. Electrical current can be derived using these two standards via Ohm's law, however, a direct independent measurement would allow for greater precision in the value and close the so called quantum metrological triangle, in which consistency between each standard can be tested. In order to do so, the error in the measured current must be smaller than the derived result, currently 10 parts per billion (0.01 ppm) [19].

In this section, previous work on single electron devices and some principles of their operation are briefly reviewed.

2.3.1 SET Device Development

The *single electron turnstile*, developed around the 1990s and based on the single electron transistor initially developed at Bell labs [21], was one of the first devices to demonstrate a controlled single electron current, with a source-drain current characteristic of Eq. 2.21 [22, 1, 23]. These devices used a small nanodot decoupled from the source and drain by tunnelling junctions and capacitively coupled (non-tunnelling) to a central electrode V_g. They work by making the purely classical Coulomb *charging energy* of the dot (the energy required for an electron to tunnel into it) $E_c = \mathrm{e}^2/C_\Sigma$, where C_Σ is the sum of the capacitances between the dot and its surroundings, large enough to create discrete energy levels (similar to an atom) between the Fermi energies of the source and drain. To achieve this, the tunnelling junctions were made ultra thin while keeping the conductance less than e^2/h (necessary to prevent electron delocalisation through the junction). At high enough E_c or low enough temperatures (such that $E_c \gg k_bT$), electrons that tunnel into the dot energetically suppress the tunnelling of other electrons by raising the electrostatic energy of the dot by E_c, establishing a *Coulomb*

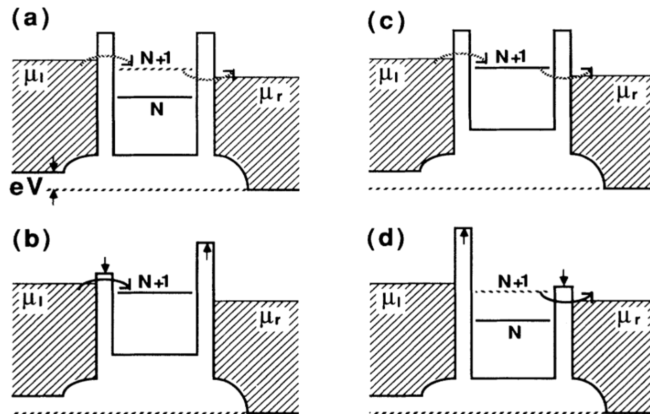


Figure 2.1: Turnstile single electron pump by Kouwenhoven et. al. [1]. **(a)** shows a vacant energy level on the dot, ready for an electron to tunnel into it as it is at a slightly lower potential than that of the left bulk reservoir. **(b)** shows an electron tunnelling onto the dot due to the left barrier being lowered. **(c)** shows the electron being trapped on the dots as both barriers are set. **(d)** shows the electron tunnelling off the dot and into right reservoir as the right barrier is lowered.

blockade. By varying the voltage on the centre gate, the conductance of the dot could be precisely manipulated, oscillating between zero, Coulomb blockaded, and non-zero. These were called *Coulomb oscillations*. Increasing the source-drain bias voltage V_{DS} would increase the number of electrons that pass through the turnstile per cycle (i.e n from Eq. 2.21). Geerlings et. al. [22] defined their dots and junctions using metallic 'islands' that were physically separated, achieving single electron current control by only oscillating V_g. Kouwenhoven et. al. [1] oscillated the tunnelling barrier potentials defining their dots in a heterostructure 2DEG, through the field effect of applied RF signals to two-finger gates, allowing electrons to tunnel into the dot, trapping them and then releasing them, as shown in Fig. 2.1.

One of the key problems with the turnstile type device was the degradation in the accuracy of the output current as the transport frequency increased, due to the inherent relation between the current and the electron tunnelling rate (a stochastic process) Γ through the device's junction barriers. Geerlings et. al. [22] showed that $\Gamma \propto (RC)^{-1}$ with the expected probability for an electron to miss a cycle being $p_m \simeq \exp(-\Gamma/f)$, therefore $f \ll (RC)^{-1}$ was required to realise a current of acceptable accuracy. Their device had $(RC)^{-1} \simeq 5\,\text{GHz}$ so at $f = 5\,\text{MHz}$, $p_m \simeq 10^{-44}$ while at $f = 50\,\text{MHz}$, $p_m \simeq 10^{-5}$ which is many orders of magnitude worse. Due to this RC factor, the pumps had to be operated at low frequencies to stay accurate, which meant only small current could be measured. A better way had to be found.

In 1992, Pothier et. al. [24] developed the first so-called *single electron pump* which was similar to the turnstile, utilising the Coulomb blockade effect, but used two RF signals applied to two finger gates capacitively coupled to two dots that periodically modulated the potentials on the dots allowing only a single electron through each cycle. The signals were phase shifted by $\pm\pi/2$ with the sign determining the direction of the current flow. No V_{DS} bias voltage was necessary unlike in the turnstile. The RF's were biased to operate around a triple-point, such that a single electron would be 'pumped' per cycle. Theoretical work done on pumps [25, 26, 27] indicated that the frequency and accuracy of the current could be made high enough to be suitable for application to metrological definitions [25]. These pumps also suppressed other parasitic processes such as electron co-tunnelling (a coherent quantum-mechanical process in which $N > 1$ electrons can tunnel through different barriers at the same time, inducing a parasitic current) as arrays of five or more junctions were used which would almost eliminate the effect [25].

In 1996, a new driving mechanism that did not rely on the Coulomb blockade effect was developed by Shilton et. al. [28] who observed the first quantised acoustoelectric transport using surface acoustic (SAW) waves, with others [29, 30, 31] improving the accuracy and frequency into the GHz range. Further developments the field of nanofabrication led Fujiwara et. al. [32] in 2004 to develop a charge-coupled device (CCD) capable of quantised transport in a fashion similar to the pumps, using three fine finger gates lying along an etched narrow Si-wire channel in which electrons were shuttled along using phase-shifted square voltage pulses. However, the device could only be operated up to 100 MHz. In 2007, Blumenthal et. al. [33] developed a device similar to Fujiwara et. al. but with only two finger gates having phase-shifted sinusoidal voltages applied to each. Electrons 'surf' as particles on the potentials instead of tunnel through junction barriers as waves, achieving a very high transport frequency of 3.4 GHz with an accuracy of 10^{-4}.

2.3.2 2DEG formation

Many of the devices from the aforementioned works used a 2DEG constructed within a semiconductor heterostructure. At the interface between two dissimilar semiconductors, a *heterojunction* forms in which the band energies of the two layers bend to meet. In the case of a doped n-type AlGaAs and GaAs interface, a sharp triangular band is formed as shown in Fig. 2.2. As electrons close to the interface move to the energetically favourable GaAs side, they lose their kinetic energy and become trapped. Due to this confinement, their movement along the z-axis becomes quantized, forming a 2DEG.

Commonly, the different layers used to construct a heterostructure are grown using a Molecular Beam Epitaxy (MBE) process, where the band

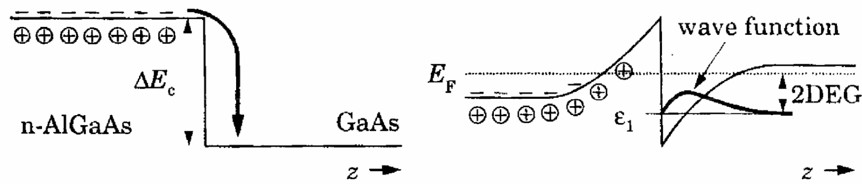


Figure 2.2: Energy band bending resulting in the confining potential for the formation of a 2DEG at a heterojunction (from [2]).

profile of the resulting structure is specifically engineered to give different properties. Of particular importance is high electron mobility in the 2DEG which yields lower scattering times and thus a more accurate current. *Modulation doping* is a technique commonly used to improve mobility, in which the n-type dopant is grown in a region away from where the 2DEG forms and at a higher band energy. The charges migrate away from their donors 'down' to the 2DEG, reducing scattering caused by the ions. A spacer layer is additionally employed to further reduce this interaction but reduces the charge density [2]. In general, the higher the density of a charge system, the lower its mobility and vice versa and is a problem that is actively worked on. Recently, mobilities in the order of 10^6 at densities of 10^{11} have been recorded [34].

2.3.3 Schottky Barriers and Ohmic Contacts

Metal gates (such as finger and spilt gates) deposited on top of the heterostructure are used to control the depletion of the 2DEG within, forming the junction barriers and quantum dots (lateral confinement is usually achieved by etching away the dopant around a very narrow 1D mesa-wire). This interface creates a metal-semiconductor (MS) junction where a high potential barrier forms, known as a *Schottky barrier*, given to a first approximation by the Schottky-Mott rule $\phi_{B0} = \phi_m - \chi$, where ϕ_m is the work function of the metal and χ is the semiconductor electron affinity [16]. Applying a negative potential to the metal gate, relative to the semiconductor, lowers the energy band in the semiconductor around the gate yet no current flows between the two due to the barrier. The lowered bands in the semiconductor cause charges from the 2DEG to migrate toward it, mediating the field effect that depletes the 2DEG below the gate.

In order to bias the 2DEG or measure its conduction, a direct electrical connection must be made to it. Ideally, this contact should have very low-resistance with little to no Schottky barrier so the current through it is a linear function of the applied voltage (thus known as an *Ohmic contact*) [16]. It is fabricated using a metallization process followed by an annealing process, in which the metal ions diffuse into the part of the heterostructure

that holds the 2DEG.

2.4 Electrons on Liquid Helium

Electrons will become bound to the surface of liquid helium due to their own induced image potential in the weakly polarizable liquid. A very clean, non-degenerate (i.e. classical) electron 2DEG forms above the interface between the liquid and vacuum. This interesting non-degeneracy is due to the largely unscreened Coulomb interactions between the electrons, as liquid helium has a small dielectric constant ($\epsilon_r \simeq 1.057$). Many other interesting quantum phenomena, not directly related to this thesis, can be studied with this system (such as investigating the topological surface structure of superfluid ^{4}He [7], Wigner crystallisation [8] and Coulomb liquids [9]).

In this section, a review of previous work in the field is given as well some of the relevant physical properties and models by which the system operates. The applicability to SET is discussed at the end.

2.4.1 Review of Relevant Literature

Sommer [5] in 1964 experientially showed that liquid helium will appear as an energy barrier of $\sim 1\,\mathrm{eV}$ to electrons, which indicated that electrons form a self-induced image potential cavity on the liquid's surface. Cole and Cohen [4, 35] followed by examining the properties of image potentials induced in the surface of insulators at low temperatures. They proposed a physical model showing that mobility parallel to the surface is nearly free-electron like and can accurately be characterized by a two-dimensional electron gas (2DEG). They also demonstrated the temperature dependence of the mobility, limited by scattering caused by quantised 'ripplons' in the liquid and atoms in the vapour. Soon after Williams, Crandall, and Willis [36] were the first who 'tentatively' used this model to explain their experiential observations of electron states above liquid helium. In 1971, Sommer and Tanner [37] devised a method for measuring the mobility of the charges using electrodes placed just underneath the top of the liquid's surface. The resulting phase shift of a signal applied to an electrode, capacitively coupled through the surface charges, could be measured and related to the charge system's mobility. At Bell labs, Brown and Grimes [38] demonstrated cyclotron resonance in these surface-bound states where Grimes and Adams [8] followed by recording the first electron-liquid to electron-crystal phase transition forming a Wigner crystal in 1979.

Marty [3] later investigated ways of improving the density of these surface state electrons (SSEs), showing that their density is limited by a hydrodynamic instability in liquid caused by the pressures exerted on its surface by the charges and other forces (refer to Sec. 2.4.3). After a critical charge density is reached, charges will begin breaking through the liquid's surface forming bubble states within it. To suppress this, Marty proposed using a 'fractionated' geometry with a periodic meander line electrode structure,

forming channels which would fill with superfluid ^{4}He by capillary action from the bulk level (see Sec. 2.4.3). Marty demonstrated that it worked and recorded a density in the order of $4 \times 10^9\,\mathrm{cm}^{-2}$, doubling the previous best of $\sim 2 \times 10^9\,\mathrm{cm}^{-2}$. Marty also noted that as the depth of the film decreases due to an increase in the charge density, the mobility of the charges also decreases. Therefore by stabilizing the film's surface, the mobility for a given charge density was increased too.

The mobilities associated with SSEs on superfluid ^{4}He are some of the highest of any physical system (in the order of 10^7cm/Vs [6]) due to the charges being well isolated above the fluid's surface. This implies SSEs will have high coherence times too, which caused much interest in the applicability of this system to quantum computing, especially as the number of electrons is highly scalable. Platzman and Dykman in 1999 [39, 40] proposed using the first two hydrogenic Rydberg energy states of each individual electron as convenient qubits, whose state can be changed by the application of a microwave field. In 2006, Lyon [10] proposed creating a spin-based qubit using pairs of electron spins to encode each qubit into a decoherence-free subspace (DFS), mitigating against noise. However, the largely unscreened electron-electron Coulomb interactions inhibit quantum exchange interactions, posing a challenge for the creation of qubits. Magnetic dipole-dipole coupling between spins, using a quantum dot and coupling the orbital state to the spin state via a magnetic field, have been suggested as a method to overcome the problem. A recent paper published in Nature Communications [41] demonstrate coupling electrons to a superconducting resonator inside a quantum dot, allowing them to leverage the field of circuit quantum electrodynamics (cQED) to interact with the electrons in the dot using microwave frequencies.

Papageorgiou et. al. [12] in 2005 used a superconducting single-electron transistor as an electrometer placed underneath the helium film to count the number of electrons trapped inside the pool above. They observed the distinctive Coulomb staircase as electrons left the dot one by one. In 2011 Bradbury et. al. [11] demonstrated precise and efficient control over the positions of electrons in channels, being able to move them by strong coupling to gate electrodes underneath the surface of the fluid, thus allowing efficient clocking of the electrons in a CCD type fashion. The work in this thesis is based on the work by Bradbury et. al., with Dr Forrest Bradbury being a collaborator in this group.

Commonly, the liquid helium surface is charged by thermal emission of electrons from a very thin (10 µm diameter) thoriated tungsten filament, flashed very briefly. The charges are attracted to the surface due to attractive potentials applied to a device's electrodes.

2.4.2 Superfluidity

The formation of superfluid ^{4}He is the somewhat remarkable manifestation of microscopic quantum phenomena becoming apparent at a macroscopic scale. At 1 atm, ^{4}He liquefies at around 4.2 K (referred to as He-I phase) and undergoes another phase transition into the superfluid phase (referred to as He-II phase) at the critical λ-point (or λ-temperature) $T_\lambda = 2.17\,\mathrm{K}$ [42, 15]. He-II exhibits incredible properties such as flowing without friction over surfaces and through tiny capillaries as it has no viscosity. It can creep up the sides of walls it is contained by, extending past the bulk level due to the adhesion to surfaces via the Van der Waals force [15].

The physics of explaining the behaviour of He-II is very involved and the question of why exactly $T_\lambda = 2.17\,\mathrm{K}$ is still an open one [42]. In 1938, London and Tisza [43] suggested the connection between He-II superfluidity and a Bose-Einstein Condensate (BEC). The basis of their argument was that at a low enough temperature, the density of the fluid will increase to a degenerate point where the average de Broglie wavelength of each atom approximately equals the interatomic distance. Due to the bosonic nature of the ^{4}He atom (having integer spin 0 as opposed to ^{3}He which is fermionic having spin 3/2), these atoms will begin obeying Bose-Einstein statistics with each atom occupying the same ground state energy. This corresponds to the collective coherent properties of the condensate and explains why ^{3}He requires a much lower temperature to turn into a condensate (requiring first Cooper pairing of the atoms followed by a condensation [44]). However, in this theory, the liquid must be treated as an ideal, non-interacting Bose gas, which is not the case, and the calculated critical temperature $T_\lambda = 3.14\,\mathrm{K}$ did not agree with experiment (but was of the same order of magnitude).

The two-fluid model proposed by Tisza [45] and refined by Landau [46] suggested that below T_λ helium consists of two components, normal and superfluid, which described the long-wavelength excitations via 'phonons' and 'rotons' for the relatively short-wavelength collective excitations [47]. More recently, theories involving the spontaneous breaking of the $U(1)$ gauge symmetry in He-II have been more successful, with [42] calculating $T_\lambda = 2.194\,\mathrm{K}$.

2.4.3 Superfluid Helium Channels

The devices used by Marty [3], van Haren et. al [48], Bradbury et. al [11] and others have horizontal periodic arrays of channels fabricated into them which fill with superfluid ^{4}He by the creeping effect due to capillary action from the bulk level, as explained in the previous section.

The following is a derivation is taken from Marty [3] and van Haren et. al. [48]. z is the perpendicular height above the fluid level in a channel. The stability of the fluid film in each channel is determined by the pressures

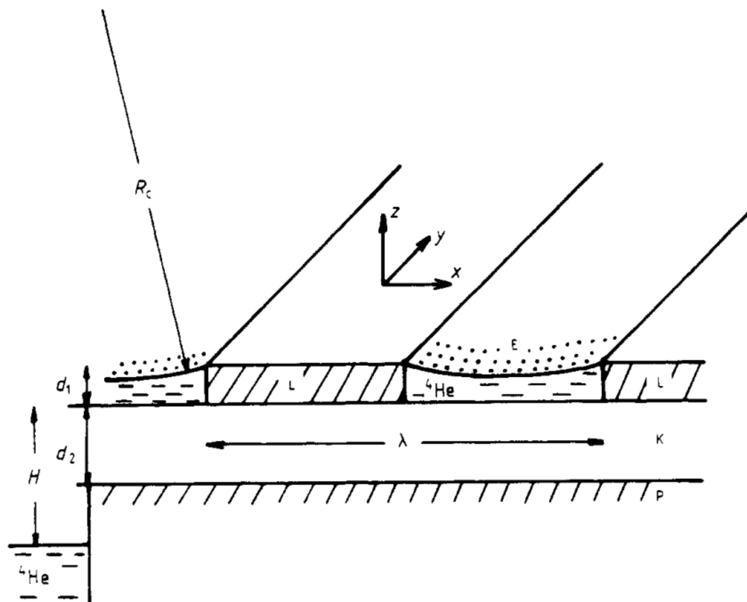


Figure 2.3: The fractionated channel geometry model used and developed by Marty [3].

exerted on it and consists of three terms:

- $\rho g z$: The hydrostatic pressure due to gravity, associated with the energy gained by the creeping (ρ is the mass density of the fluid).
- $\sigma \nabla^2_{x,y}\, z$: The pressure due to surface tension σ.
- $-(n_s^2 \mathrm{e}^2/\epsilon_{\mathrm{He}})\nabla_{x,y}\, z$: The pressure due to the mutual repulsion of the electrons given in [3] (n_s is the areal surface charge density).

Taking the spatial Fourier transform of this pressure gives

$$P(\mathbf{k}_{\|}) = \begin{bmatrix} P(\mathrm{k}_x) \\ P(\mathrm{k}_y) \end{bmatrix}\,, \tag{2.22}$$

where

$$P(\mathrm{k}) = (\sigma \mathrm{k}^2 - (n_s^2 \mathrm{e}^2/\epsilon_{\mathrm{He}})\mathrm{k} + \rho g) Z(\mathrm{k})\,, \tag{2.23}$$

which is an expression for the spatial frequency of the pressure deformations in the x, y-plane parallel to the surface due to changes in the pressure acting upon it. $Z(\mathrm{k})$ is the Fourier transform of the vertical displacement z above the fluid's surface in a channel.

The hydrodynamic stability condition for the surface being that this quadratic remains positive for all k (in that direction), implying the discriminant must remain negative (giving only complex roots)

$$(n_s^2 \mathrm{e}^2/2\epsilon_{\mathrm{He}})^2 - \rho g \sigma \leq 0\,, \tag{2.24}$$

from which an expression for the critical density (the density after which the fluid film can no longer hold the charges) $n_{s,c}$ can be found:

$$n_{s,c} = (\rho g \sigma)^{1/4}/(\mathrm{e}^2/2\epsilon_{\mathrm{He}})^{1/2} \to 2.25 \times 10^9\,\mathrm{cm}^{-2}\,, \tag{2.25}$$

with $\rho = 0.145\,\mathrm{g/cm^3}, \sigma = 0.378 \times 10^{-3}\mathrm{N/m}$ for superfluid ^{4}He below 1.4 K [3].

Although superfluid ^{4}He has zero viscosity (as the fluid considered to be one large composite-boson, with all ^{4}He atoms occupying the same quantum state), this does not imply that the fluid has no surface tension, which is implicitly defined for all interfaces between two different materials (or phases of a single material). Lu [49] develops expressions for the surface tension of and discusses the mechanics of the zero viscosity fluid in more detail.

As shown by Marty, one could use a periodic array of channels to impose a limit on the minimum allowable wave-vector in a single direction $\mathrm{k_{min}} \simeq \pi/w$ (w is the width of the channel), making the stability condition

$$\sigma \mathrm{k}_{\mathrm{min}}^2 - (n_s^2 \mathrm{e}^2/\epsilon_{\mathrm{He}})\mathrm{k}_{\mathrm{min}} \geq 0\,, \tag{2.26}$$

(the ρg term is dropped as $k_m \gg \rho g$ for channels with widths in the order of µm), increasing the critical density to

$$n_{s,c} = \left[\frac{\sigma k_{\mathrm{min}} \epsilon_{\mathrm{He}}}{\mathrm{e}^2}\right]^{1/2} = \left[\frac{\sigma \pi \epsilon_{\mathrm{He}}}{w \mathrm{e}^2}\right]^{1/2}\,, \tag{2.27}$$

now a function of channel width w.

The radius of curvature of the superfluid ^{4}He surface in a channel is given by Jurin's law [3, 48]:

$$R_c(n_s) = \frac{2\sigma}{\rho g H + \mathrm{e}^2 n_s^2/(\epsilon_{\mathrm{He}})} \simeq \frac{2\sigma\epsilon_{\mathrm{He}}}{n_s^2 \mathrm{e}^2}\,, \tag{2.28}$$

where H is the distance from the bulk level to the top of the channel as shown in Fig. 2.3 and $n_s \gg H$.

The minimum depth of the fluid's surface in the channel is given by [3, 48]

$$d_0(n_s) = h - \frac{w^2}{8\sigma}\frac{\mathrm{e}^2}{2\epsilon_{\mathrm{He}}} n_s^2\,, \tag{2.29}$$

where h is the channel height (d_1 in Fig. 2.3).

2.4.4 Surface State Localisation

An electron above a liquid ^{4}He film will become trapped due to approximately two potentials: the short-range repulsive energy barrier of the film of approximately $V_0 \simeq 1\,\mathrm{eV}$ (established by the Pauli exclusion principle preventing an electron from occupying an orbital of a neutral ^{4}He atom) and

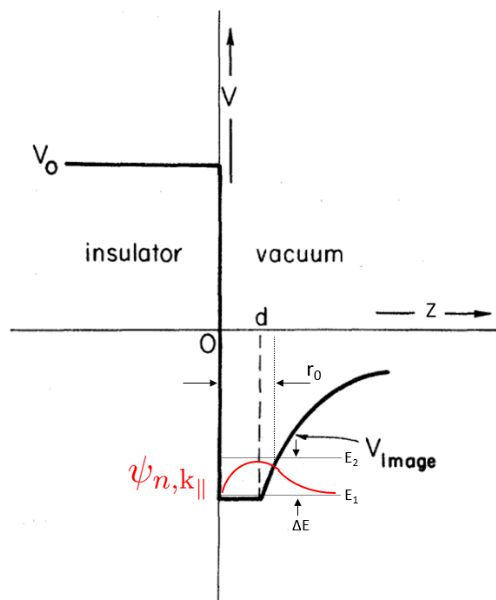


Figure 2.4: Electron wave-function (in red) inside the self-induced image potential in the liquid's surface, adapted from Cole and Cohen [4].

the induced image potential in the film due to the weakly polarizing effect of the electron V_{image} (Eq. 2.30).

The following derivation is taken from Cole and Cohen [4], Platzman [39]. The z-direction is taken to be the perpendicular ($\perp$) distance from film's surface and the x, y-directions parallel ($\|$) to it. By the method of images, the potential of an electron in the vacuum above a flat liquid helium film is given by [4]

$$V_{\text{image}}(z) = -\frac{\Lambda \mathrm{e}^2}{z}, \tag{2.30}$$

$$\Lambda = \frac{1}{4} \cdot \frac{\epsilon_{\text{He}} - 1}{\epsilon_{\text{He}} + 1}. \tag{2.31}$$

This assumes the surface of the film is flat, which is not exactly the case as a small cavity is developed in the film due to the electron repulsion, slightly lowering the zero-point energy of the image potential. Also the curvature of the film given by Eq. 2.28 has no effect at the scale of an electron.

This image potential formulation (Eq. 2.30) becomes inadequate for $z < d$, where d is in the order of one interatomic distance and the potential is given by a constant V_1. Thus, the perpendicular potential is described by the

following, as shown in Fig. 2.4:

$$
\begin{aligned}
V_\perp(z) &= V_0, \quad z \leq 0\,, \\
&= -V_1 = -\frac{\Lambda \mathrm{e}^2}{d}, \quad 0 < z \leq d\,, \\
&= V_{\mathrm{image}}(z) = -\frac{\Lambda \mathrm{e}^2}{z}, \quad z > d\,.
\end{aligned}
\tag{2.32}
$$

With no confining potentials in the parallel x, y-plane, the TISE (Eq. 2.1) can be written for this system using the effective mass approximation to separate the parallel and perpendicular directions as follows

$$
\left[-\frac{\hbar^2}{2\mathrm{m}_\parallel}\nabla^2_{x,y} - \frac{\hbar^2}{2\mathrm{m}_\perp}\frac{\partial^2}{\partial z^2} + V_\perp(z)\right]\psi = E\psi\,, \tag{2.33}
$$

where

$\mathrm{m}_\parallel$ is the parallel component of the electron's mass,

$\mathrm{m}_\perp$ is the perpendicular component of the electron's mass.

The solutions are

$$
\psi_{n,\mathbf{k}_\parallel}(\mathbf{p}, z) = e^{i\mathbf{k}_\parallel\cdot\mathbf{p}}\varphi_n(z)\,, \tag{2.34}
$$

$$
E_n(\mathbf{k}_\parallel) = \frac{\hbar^2}{2\mathrm{m}_\parallel}|\mathbf{k}_\parallel|^2 + E_n\,, \tag{2.35}
$$

where

$\mathbf{p}$ is the position vector in the x, y-plane parallel to the film,

$\varphi_n(z)$ is the perpendicular wave function with energies, E_n, solved for below.

This result shows that a 2DEG forms in the plane parallel to fluid's surface.

It follows that for $z > d$ [4]

$$
-\frac{\hbar^2}{2\mathrm{m}_\perp}\frac{\mathrm{d}^2}{\mathrm{d}z^2}\varphi_n(z) - \frac{\Lambda \mathrm{e}^2}{z}\varphi_n(z) = E_n\varphi_n(z)\,. \tag{2.36}
$$

This is identical in form to a radial TISE for the Coulomb potential of an atom with a nucleus of charge of Λe.

In the limit as $d \to 0$ and $V_0 \to \infty$, approximate solutions are found to be equivalent to hydrogenic Rydberg energy levels [4]

$$
E_n = -\frac{m_\perp \mathrm{e}^4}{2\hbar^2}\left[\frac{\Lambda}{n}\right]^2 = -\mathrm{R}\left[\frac{\Lambda}{n}\right]^2\,. \tag{2.37}
$$

Here $m_\perp$ is taken to be the free-electron mass $\mathrm{m_e}$ and $\mathrm{R} = 13.6\,\mathrm{eV}$ is the Rydberg energy.

Thus, for a stationary electron ($\mathbf{k}_\parallel = 0$) above the film's surface, its approximate ground-state energy is $E_1 \simeq -0.7\,\text{meV} \to 8.1\,\text{K}$ and the first excited state is $E_2 \simeq -0.16\,\text{meV} \to 1.9\,\text{K}$, for splitting energy of $\Delta E = 0.54\,\text{meV} \to 6.2\,\text{K}$. This is much higher than the temperature needed for superfluid ^{4}He ($\sim 2.17\,\text{K}$, refer to Sec. 2.4.2) meaning most electrons will be frozen into the ground state given sufficient time for thermalisation.

The expectation value of the perpendicular distance for the ground-state from the fluid's surface is approximately given by an effective Bohr radius of $\langle z \rangle_{\varphi_0} = r_0 = \hbar^2/\mathrm{m_e e^2}\Lambda \simeq 100\,\text{Å}$.

2.4.5 Transport

The work by Bradbury et. al. [11] demonstrated precise and efficient control over the position of packets of charges along superfluid ^{4}He channels. In a similar fashion to the way a 3-phase Charge-Coupled Device (CCD) [50] works, the charges were moved along the channels by the application of time-varying potentials to electrodes beneath. A central gate would become more attractive with respect to the gates on either side of it, moving the charges towards it. This would be done to each successive gate along the length of a channel, giving a precise way to control the positions of the packets of charges.

The movement of charges in this fashion is extremely efficient as there is very little scattering, given that each charge is well isolated above the surface (as explained in the previous section). Predominantly, scattering events are caused by interactions with quantised ripplons in the superfluid and ^{4}He atoms in the vapour phase above the surface. Bradbury et. al. report no measurable signal loss after transporting charges at a frequency of 240 kHz for over a billion cycles. They were able to additionally show 2D transport by shuttling the charges along a perpendicular channel, deterministically removing a single charge at a time and measuring the reduction in the signal until there were no charges left.

2.4.6 Charge Detection and Measurement

The foundational work by Sommer and Tanner [37] demonstrated a non-destructive, capacitive sensing approach to measuring the mobility of charges on the surface of liquid ^{4}He, which is now simply called the Sommer-Tanner method. They modelled the system as a sheet of electrons (like a conductive metal plane) sharing a per unit length capacitance C with electrodes beneath the surface and a per unit length resistance R along the surface. This resistance could be related to the system's mobility as $R \propto \sigma^{-1}$, with the conductivity $\sigma = \mu C V_e$, where V_e is the potential of the system at the surface and μ is the mobility.

By applying an ac driving potential to a 'twiddle' gate, the difference

in the phase of the induced potential on a 'sense' gate between the charged and uncharged surface can be measured. By using the RC relationship on the system, the mobility can be determined. It is important to note the resistance R is caused by a lag in the movement of a large total number of charges due to diffusion along the path travelled in response to the oscillating electric field.

Bradbury et. al. [11] used a similar capacitive sensing technique, but had far fewer charges being sensed per cycle with small packets of charges per channel and 120 channels in total. Because of this, and the relativity short distances travelled per sensing cycle, the equivalent circuit model was different and the quantity of interest measured was rather the change in the magnitude of the induced potential on the sense gate, instead of the phase difference (refer to Sec. 3.2.2 for a full mathematical model).

2.4.7 Application to SET

The high mobility exhibited by charges above superfluid ^{4}He at non-degenerate densities presents an opportunity to explore single-electron transport in a new and interesting regime.

Using the deterministic transport technique demonstrated by Bradbury et. al. [11] and the largely unscreened Coulomb interactions between the electrons, a quantum dot with a large charging energy could be established in this system. A single electron turnstile, similar to those used in the early work by Kouwenhoven et. al. [1], could therefore be implemented (refer to Sec. 3.2.3 for a full model and explanation).

One of the main challenges with this approach is the inability to make direct contact with the charge system. This makes an Ohmic contact impossible to create which prevents direct current measurements. A possible approach to solving this may be to use a gate that allows charges to tunnel into it if a sufficiently attractive potential is applied to it. This has not yet been shown and is one of the goals of this project.

CHAPTER 3

DEVICE DESIGN AND FABRICATION

3.1 Overview

Fig. 3.2 shows the device with all six of the lithography layers together, each colour representing a different layer. The gates are numbered 1-22 with descriptions of each given in Table 3.1. Fig. 3.3 shows the central part of the device, with a close-up of the critical section showing how the channels (in blue) relate to the bottom gates (in red).

Dr Forrest Bradbury was responsible for the initial design, defining the geometry of the channels and gates and functionality of the device as a whole. These designs were based on the devices he used in his PhD at Princeton University.

The fabrication was done at the Centre for Nanophase Material Science (CNMS) in Oak Ridge National Labs (ORNL), a federal research facility in the USA that collaborates with research groups from around the world, giving them access to the cleanroom and other facilities they have, free of charge (for which I am deeply grateful).

I was primarily responsible for developing the fabrication process, attached as an appendix (App. A), and iterating on the design of the device. This involved spending a cumulative total of 5 weeks in the cleanroom, split between an initial 2-week visit followed later by a 3-week visit, conducting various tests and experiments and using the results to develop the process and modify and adding to the design as needed. This included performing various Finitie Element Modelling (FEM) analyses to determine various fabrication parameters and tolerances.

Jacob Swett, a highly experienced cleanroom user at CNMS, was a collab-

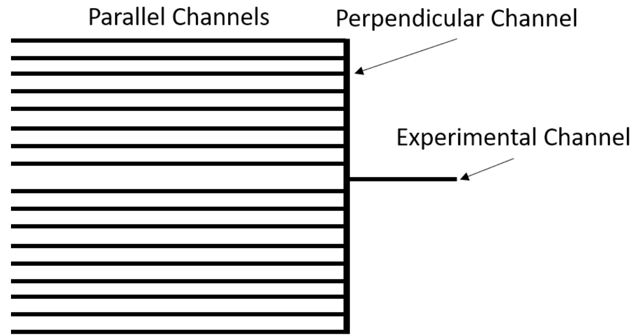


Figure 3.1: A simplified diagram of the centre of the device showing the three main channel regions.

orator in the group and provided immensely useful guidance and instructive help regarding the fabrication. Ivan Kravchenko and Nickolay Lavrik, both staff scientists at CNMS, collaborated with our group and provided their expertise.

The central part of the device consisted of three main channel regions shown in Fig. 3.1:

- **Parallel Channels** - 120 channels running parallel to each other. These channels were used for charge collection and had a set of turnstile and capacitive charge sensing gates that ran beneath the channels.
- **Experimental Channel** - A single channel used to precisely control just a single line of charge. It too had a set of turnstile and capacitive charge sensing gates.
- **Perpendicular Channel** - A singular channel connecting the parallel channels to the experimental channel.

The superfluid ^{4}He fills the channels due to its ability to creep up the sides of walls from its bulk level, kept relativity close to the device.

The primary functional goal of the device was to be able to clock a set amount of charge through the turnstile gates and be able to measure the amount of charge that was clocked through using the capacitive charge sensing gates. If the measured value fell within the uncertainty limits of the predicted amount of charge clocked through, then we could be sure that we did indeed achieve quantised single electron transport and that the charge measurement was accurate.

An additional goal was to drain the clocked charge away and measure a current that corresponded to the predicted value and the measured value of charge, via an ohmic contract.

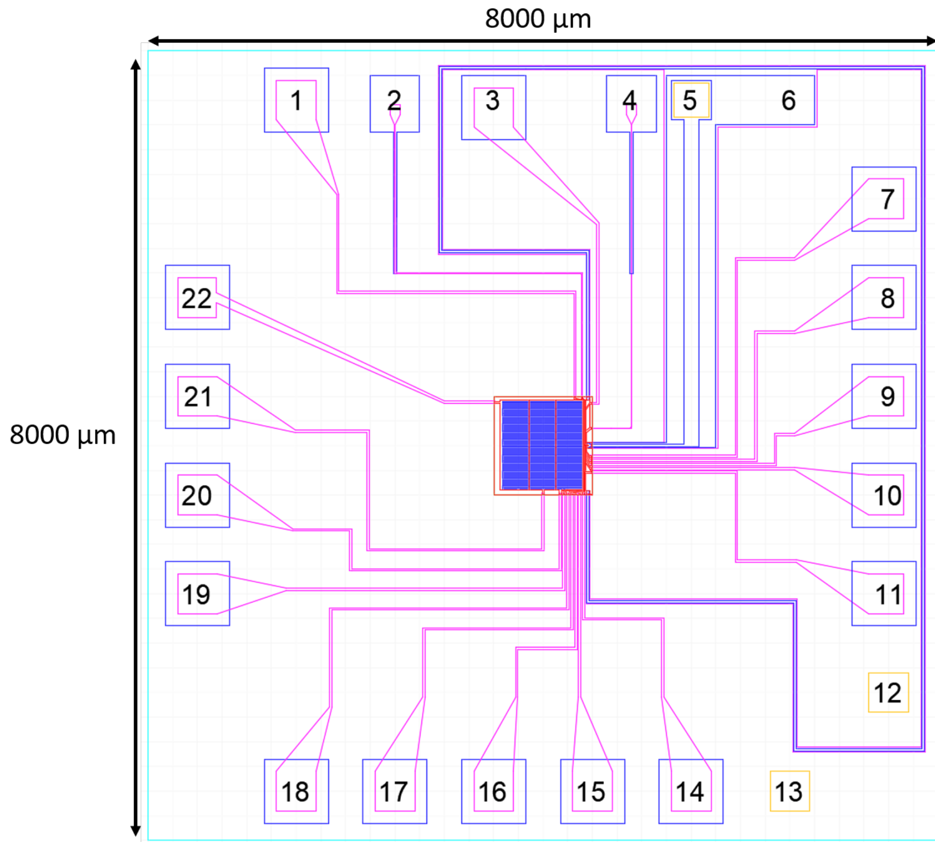


Figure 3.2: The complete device with all six lithography layers shown together, each colour representing a different layer. The square areas around the edge are bond-pads, used to make a connection to the PCB that holds the device. The traces that connect the bond-pads to the main central part of the device are coloured in magenta. The gates are numbered [1-22] with the gate types given in Table 3.1. Sec. 3.4 has the full design of each layer.

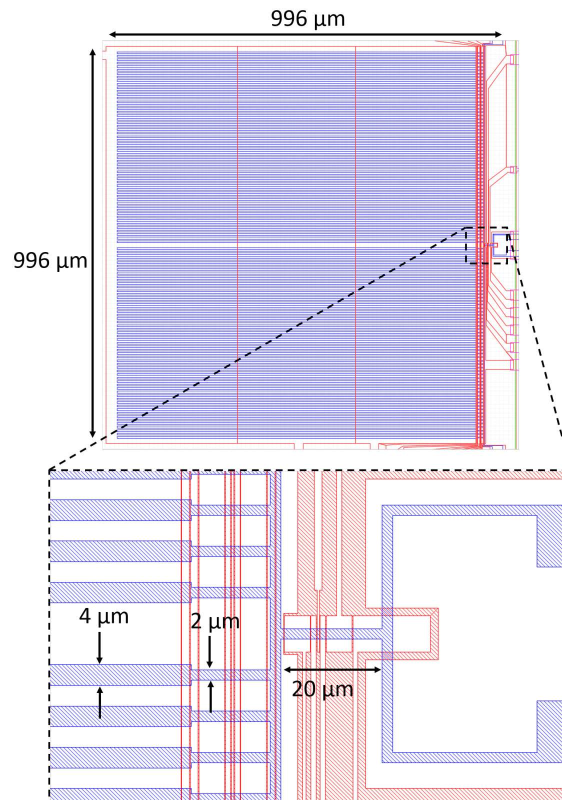


Figure 3.3: The CAD model for the central part of the device, with a close up of the experimental channel. The channels are in purple and the bottom gates are in red.

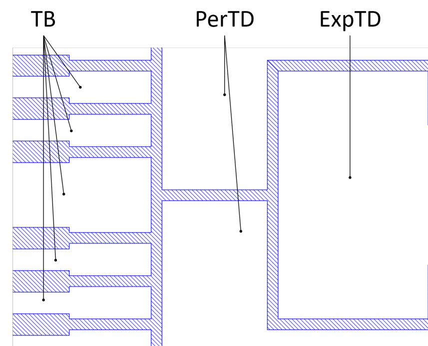


Figure 3.4: Close up of the critical region of the device, showing the three top gates.

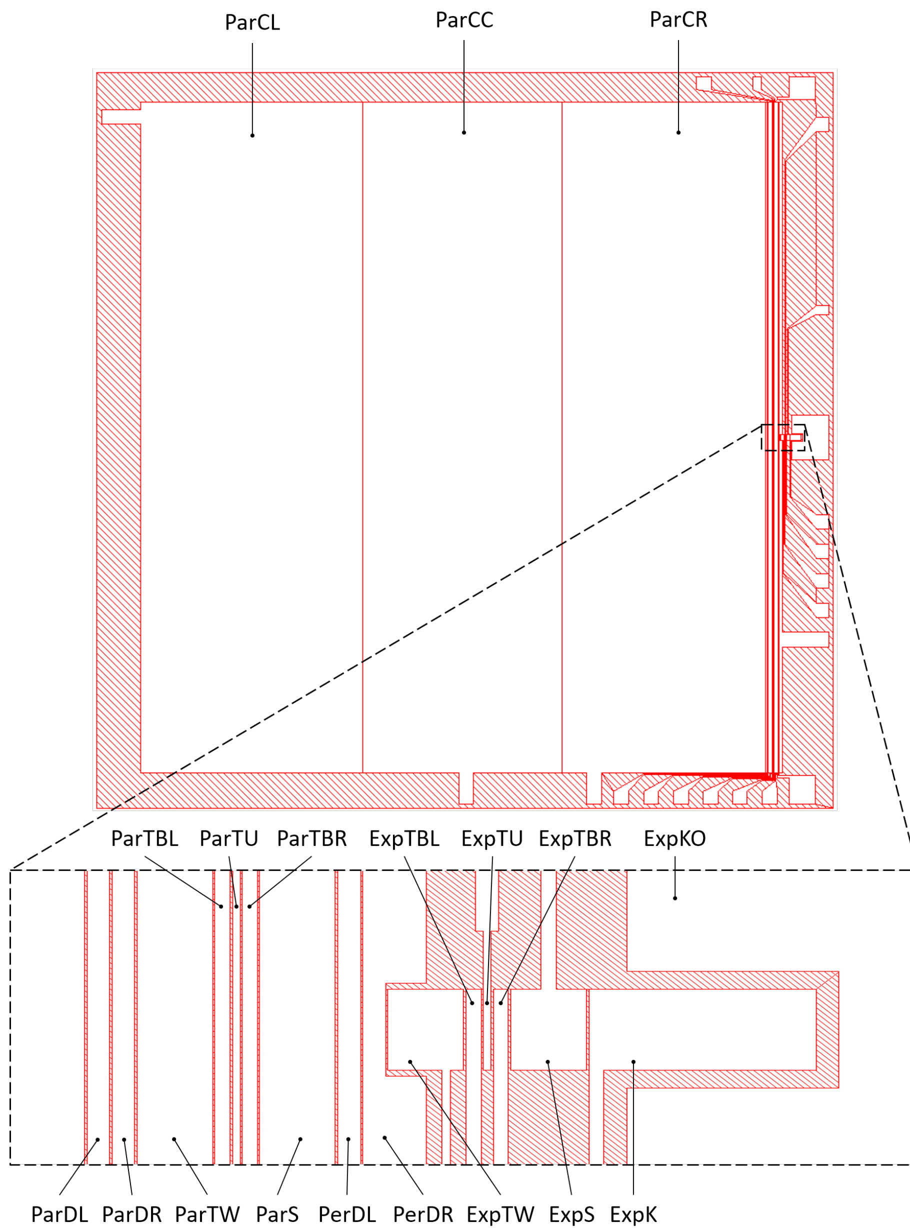


Figure 3.5: The bottom gates and their labels as defined in Table 3.1, with a zoom of the critical section.

Gate #	Acronym	Type
13	**TB**	Top Bias
	Parallel Channel Gates	
1	**ParTU**	Turnstile
2	**ParS**	Sense
15	**ParTBR**	Turnstile Barrier Right
16	**ParTBL**	Turnstile Barrier Left
17	**ParTW**	Twiddle
18	**ParDR**	Door Right
19	**ParDL**	Door Left
20	**ParCR**	Reservoir Collection Right
21	**ParCC**	Reservoir Collection Centre
22	**ParCL**	Reservoir Collection Left
	Perpendicular Channel Gates	
11	**PerP**	Pull
12	**PerTD**	Top Drain
14	**PerD**	Door
	Experimental Channel Gates	
3	**ExpTU**	Turnstile
4	**ExpS**	Sense
5	**ExpTD**	Top Drain
6	**ExpKO**	Keep Out
7	**ExpK**	Keep
8	**ExpTBR**	Turnstile Barrier Right
9	**ExpTBL**	Turnstile Barrier Left
10	**ExpTW**	Twiddle

Table 3.1: The device gate numbers, abbreviations and types.

Fig. 3.5 shows a labelled diagram of the bottom gates. The gates are prefixed according to the channels they relate to: parallel (**Par***), perpendicular (**Per***) and experimental (**Exp***).

There are five distinct functional groups:

- The reservoir collection gates (**ParCL, ParCC, ParCR**) are large, maximising their collection ability (modelling in Sec.3.2.1 explains).
- The charge sensing gates (**ParTW, ParS, ExpTW, ExpS**) are used to measure the amount of charge present in the sensing region above the gates (modelling in Sec.3.2.2 explains).
- The turnstile gates (**ParTU, ExpTU**) along with the barrier gates (**ParTBL, ParTBR, ExpTBL, ExpTBR**) on the left and right side of them, deterministically allow a single electron through per cycle (modelling in Sec.3.2.3 explains).
- The door gates (**ParDL, ParDR, PerDL, PerDR**) isolated different sections of the device, pulling charges into certain channels or preventing them from doing so.
- The Keep **ExpK** gate was designed to store charge after being sensed in the experimental channel and the KeepOut **ExpKO** gate acts to prevent charges from escaping down the lines.

Fig. 3.4 shows a close-up of the experimental channel region, with the labels for the three top gates. Their functions are:

- The top bias gate (**TB**) controls the potential at the top of the channels and confines charges into the middle of them.
- The top drain gates (**PerTD, ExpTD**) drain charges out of the perpendicular and experimental channels, by applying a sufficiently attractive potential to them so that the charges would tunnel into them and be drained away as standard current.

3.2 Modelling

3.2.1 Surface potential and charging

In general, the net electrostatic potential or voltage at some point in space in the vicinity of electrodes can be determined by adding the potential contribution of each electrode at that point in space. This point can be thought of as being capacitively coupled to those electrodes.

In applying this to our system, let the **uncharged** (i.e. when no electrons are present) potential of the surface be V_u and assume it is equipotential throughout the area we are considering. Because we are focusing on what

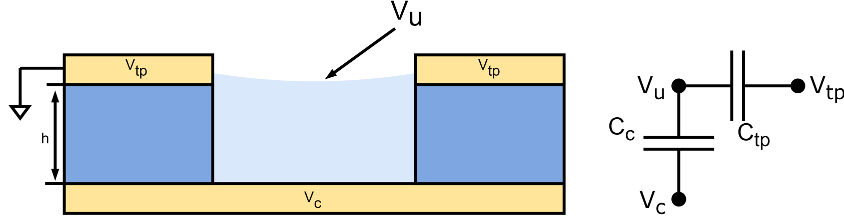


Figure 3.6: *Left*: A diagram of the system above a collection gate, along a channel, used to attract charges to the surface. *Right*: The equivalent circuit model showing the respective voltages and couplings.

happens during surface charging (also called surface loading), this analysis will focus on the charge collection regions of the device in which large collection gates have positive potentials applied to them, attracting electrons to the surface above them.

The unchanged surface potential V_u is given by

$$V_u = \frac{C_c}{C_\Sigma} V_r + \frac{C_{tp}}{C_\Sigma} V_{tp}\,, \tag{3.1}$$

$$C_\Sigma = C_c + C_{tp}\,, \tag{3.2}$$

where

$V_c\,, C_c\,,$ are the voltage of the collection gate and its coupling to the surface,

$V_{tp}\,, C_{tp}\,,$ are the voltage of the surrounding top metal, which is set as the reference ground, and its coupling to the surface.

Because V_{tp} is set as the reference ground, Eq. 3.1 reduces to

$$V_u = \frac{C_r}{C_\Sigma} V_r = \alpha V_c\,, \tag{3.3}$$

where $\alpha = C_r/C_\Sigma$ is the coupling strength of the collection gates to the surface. Using FEM analysis, V_u was found to be roughly the average between the voltage of the collection gate and the top metal, implying $\alpha \simeq 0.5$.

After a total amount of charge $Q_e = -ne$ (n is the total number of electrons in the charge system) develops on the fluid's surface, after being thermally emitted from a tungsten filament placed above, the potential of the now **charged** surface (which is the potential of the 2DEG charge system) V_e is given by

$$V_e = V_u + \frac{Q_e}{C_\Sigma} = \alpha V_c + \frac{Q_e}{C_\Sigma} = \alpha V_c - \frac{ne}{C_\Sigma}\,, \tag{3.4}$$

where the $1/C_\Sigma$ factor comes from the definition of capacitance at the surface (where for every Coulomb of electrons added to the surface, V_e will decrease by $1/C_\Sigma$).

It is fair to assume that the charges in the 2DEG are uniformly distributed over the surface area A of the fluid's surface, making $n = An_s$ where n_s is the *areal* surface charge density (i.e. the number of electrons per m^2).

The 2DEG can now analogously be thought of as a metal plate (as it has a uniform charge distribution and is equipotential throughout) which couples most strongly to the parallel plate underneath it, the large collection gate electrode.

Therefore $C_\Sigma = C_r = A\epsilon_{\text{He}}/h$ for the charge system, where $\epsilon_{\text{He}} = 9.36 \times 10^{-12}\,\text{F/m}$ is the permittivity of liquid ^{4}He and h is the height the 2DEG is above the collection gate and is equal to the depth of the fluid in the channels. Although the 2DEG is 100 Å above the fluid film, as described in Sec. 2.4.4, it can be ignored as it is negligible compared to h.

The changed surface potential V_e can now be rewritten as

$$V_e = \alpha V_c - \frac{An_s\text{e}}{A\epsilon_{\text{He}}/h} = \alpha V_c - \frac{hn_s\text{e}}{\epsilon_{\text{He}}}\,. \tag{3.5}$$

To find the maximum surface charge density $n_{s,max}$ that can develop, we need to determine when V_e will be at the same potential as the top gates V_{tp} (i.e. when $V_e = V_{tp} = 0\,\text{V}$). When this occurs, any additional charges added to the surface would make V_e negative and repelling the charges away.

By Eq. 3.5,

$$V_e = 0 \rightarrow \alpha V_c - \frac{hn_s\text{e}}{\epsilon_{\text{He}}} = 0$$
$$\therefore n_{s,max} = \frac{\alpha\epsilon_{\text{He}}}{h\text{e}}V_c\,. \tag{3.6}$$

3.2.2 Charge Sensing

As described in the theory section (Sec. 2.4.6) the total amount of charge above the surface can be determined using the Sommer-Tanner method, a non-destructive, capacitive charge sensing technique. It is achieved by applying an ac driving signal V_{tw} at frequency f_{tw} to a 'twiddle' gate beneath the surface, which induces a signal V_s on a 'sense' gate lying in the same plane (depicted in Fig. 3.8).

As the charges are moved back and forth between the two gates, a small additional potential is induced in the sense gate that can be detected using a lock-in amplifier, set to track at f_{tw}. This induced voltage is pre-amplified using a High Electron Mobility Transistor (HEMT), placed as close as possible to the device to reduce noise and any parasitic capacitance in the line

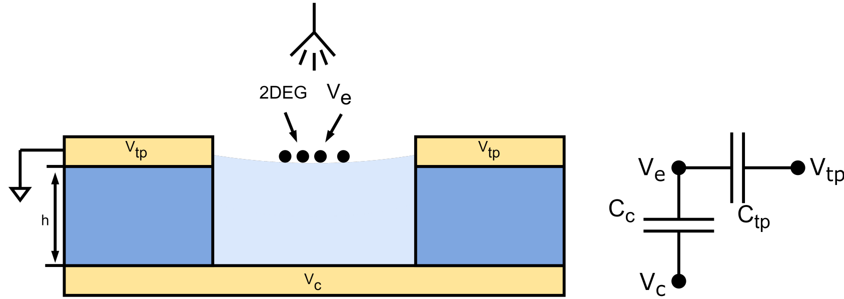


Figure 3.7: *Left*: A diagram of the system above a collection gate, along a channel, used to attracted charges to the surface. *Right*: The equivalent circuit model showing the respective voltages and couplings.

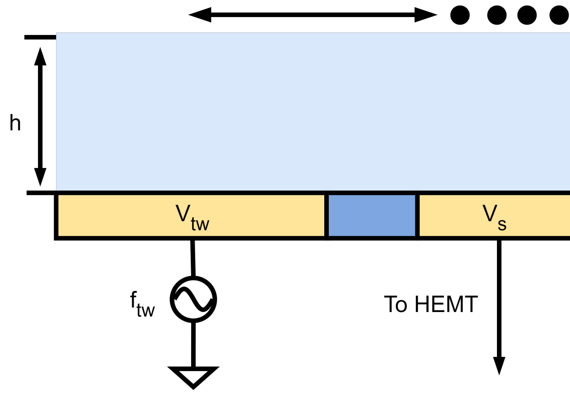


Figure 3.8: A diagram of the capacitive charge sensing part of the device. See Fig. 3.9 for the full circuit model.

connecting the two. Fig. 3.9 shows the equivalent circuit model for this system.

To derive an expression for the total number of charges present, a Laplace RC analysis is performed to find the induced potential in the sense gate (refer to Fig. 3.9).

The output impedance Z_o is

$$Z_o = \frac{R_o}{1 + R_o C_{gs} s} \,, \tag{3.7}$$

where R_o is a pull-down resistor and C_{gs} is the HEMT's gate-to-source input capacitance.

With the impedance in each line being

$$Z_{tws} = \frac{1}{sC_{tws}} \,, \; Z_{tps} = \frac{1}{sC_{tps}} \,, \; Z_{es} = \frac{1}{sC_{es}} \,, \tag{3.8}$$

where s is the Laplace variable and C_{tws}, C_{tps}, C_{es} are the relevant couplings to the sense gate.

First consider the case when no charges are present in the sensing region ($\Delta V_e = 0$). The current in the sense gate i_s will be induced by potentials applied to the surrounding gates. From Kirchhoff's Current Law (KCL):

$$i_{tp} + i_{tw} = i_s \rightarrow \frac{V_{tp} - V_s}{Z_{tps}} + \frac{V_{tw} - V_s}{Z_{tws}} = \frac{V_s}{Z_o} . \tag{3.9}$$

As in the previous model, V_{tp} is taken as the referenced ground, thus the sensed signal *before* charges are present ($V_{s,b}$) is given by

$$V_{s,b} = \frac{1/Z_{tws}}{1/Z_{tws} + 1/Z_{tps} + 1/Z_o} V_{tw} . \tag{3.10}$$

After substituting for the impedances, we find

$$V_{s,b} = \frac{R_o C_{tws} s}{1 + R_o(C_{tws} + C_{tps} + C_{gs})s} V_{tw} \tag{3.11}$$

$$= \frac{R_o C_{tws} s}{1 + R_o C_\Sigma s} V_{tw} . \tag{3.12}$$

where $C_\Sigma = C_{tws} + C_{tps} + C_{gs}$.

With the Fourier transform found by setting $s = j2\pi f$

$$V_{s,b}(f) = \frac{R_o C_{tws}(j2\pi f)}{1 + R_o C_\Sigma(j2\pi f)} V_{tw} . \tag{3.13}$$

The final reading of this signal is the output from a lock-in amplifier, which gives the magnitude of it at the reference frequency. Knowing that the twiddle gate signal and the lock-in reference are the same (i.e. $V_{ref}(t) = V_{tw}(t) = \sin(2\pi f_{tw} t)$) and if a high enough twiddle frequency is used and the output resistance R_o is large enough, both of which we have easy control over, this magnitude is simply

$$|V_{s,b}(f)|_{f=f_{tw}} = \frac{C_{tws}}{C_\Sigma} . \tag{3.14}$$

Now, after ΔQ_e of charge becomes present in the sensing region, the surface potential will increase by $\Delta Q_e/(C_{et} + C_{es})$ and oscillate at f_{tw} (because it is being driven by the twiddle gate). Although the C_{et}, C_{es} couplings change as the charges move between the gates, we only consider the system when the charges are directly above the sense gate, meaning C_{et} will be significantly less than C_{es}, thus let this signal be defined as

$$\Delta V_e = \frac{\Delta Q_e}{C_{es}} V_{tw} . \tag{3.15}$$

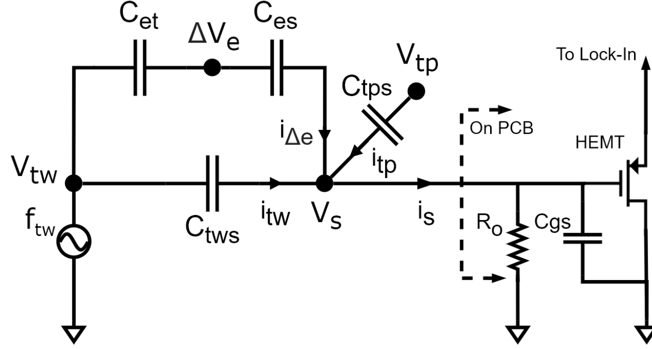


Figure 3.9: The equivalent circuit model for the capacitive charge sensing part of the device. The couplings between the 2DEG and the twiddle and sense gates are modelled by C_{et} and C_{es} respectively. The increase in the potential at the surface above the sense gate due to the 2DEG is modelled by ΔV_e. The couplings between the twiddle gate and top metal to the sense gate are modelled by C_{tws} and C_{tps} respectively. The potentials applied to the twiddle and top metal gates are given by V_{tw} and V_{tp}, with f_{tw} representing the frequency of the twiddle gate signal. V_s is the voltage induced in the sense gate, with each component current flowing into it representing the current induced from each source, with i_s being the total current induced in the sense gate. The chosen pull resistor and the input capacitance of the chosen HEMT are depicted by R_o and C_{gs}. These are both on the PCB.

This induces an additional current $i_{\Delta e}$ in the sense gate, thus

$$i_{\Delta e} + i_{tp} + i_{tw} = i_s \rightarrow \frac{\Delta V_E - V_s}{Z_{es}} + \frac{V_{tp} - V_s}{Z_{tps}} + \frac{V_{tw} - V_s}{Z_{tws}} = \frac{V_s}{Z_o}\,. \quad (3.16)$$

Therefore, the potential of the sense gate *after* charges are present ($V_{s,a}$) is

$$V_{s,a} = \frac{1/Z_{es}}{1/Z_{es} + 1/Z_{ts} + 1/Z_{tps} + 1/Z_o}\Delta V_e \quad (3.17)$$

$$+ \frac{1/Z_{ts}}{1/Z_{es} + 1/Z_{ts} + 1/Z_{tps} + 1/Z_o}V_{tw}\,. \quad (3.18)$$

Because the coupling between the charges and the sense (C_{es}) gate is very small ($1/Z_{es} \simeq 0$), $V_{s,a}$ can be given as

$$V_{s,a} \simeq \frac{1/Z_{es}}{1/Z_{ts} + 1/Z_{tps} + 1/Z_o}\Delta V_e + V_{s,b}\,. \quad (3.19)$$

After substituting for the impedances, the Fourier transform can be found

$$V_{s,a}(f) \simeq \frac{R_o C_{es}(j2\pi f)}{1 + R_o C_\Sigma(j2\pi f)}\Delta V_e + V_{s,b}(f)\,. \quad (3.20)$$

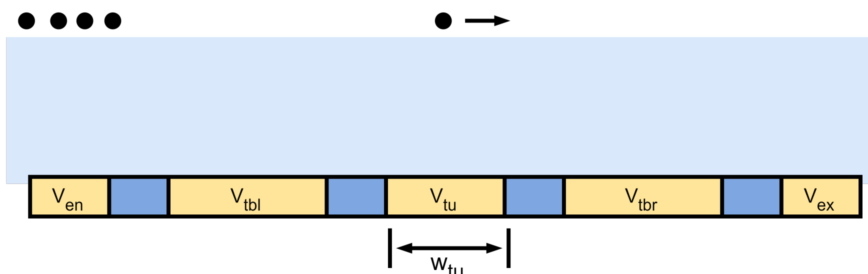


Figure 3.10: A diagram of the turnstile gates, showing the central 'turnstile' gate with two barrier gates on the left and right of it and the two entrance and exit reservoir gates. Fig. 3.12 shows how pumping through these gates would work.

Thus the final reading of this signal from the lock-in amplifier will be (using the same assumptions as before)

$$|V_{s,a}(f)|_{f=f_{tw}} \simeq \frac{C_{es}}{C_{\Sigma}} \cdot \frac{\Delta Q_e}{C_{es}} + \frac{C_{tws}}{C_{\Sigma}} = \frac{\Delta Q_e}{C_{\Sigma}} + \frac{C_{tws}}{C_{\Sigma}} . \quad (3.21)$$

Therefore by subtracting the baseline reading $|V_{s,b}|$ from $|V_{s,a}|$, we find

$$\Delta V = |V_{s,a}(f)|_{f=f_{tw}} - |V_{s,b}(f)|_{f=f_{tw}} \simeq \frac{\Delta Q_e}{C_{\Sigma}} , \quad (3.22)$$

which is the expected increase in the magnitude of the signal after ΔQ_e of charge is sensed.

If we assume the HEMT's input capacitance dominates over the other capacitances such $C_{\Sigma} \simeq C_{gs} \simeq 1\,\text{pF}$ and one electron is present in all 120 channels, the expected increase in the magnitude of the sensed signal will be

$$\Delta V = 120 \cdot \frac{1.6 \times 10^{-19}\,\text{C}}{1\,\text{pF}} = 19.2\,\mu\text{V} . \quad (3.23)$$

3.2.3 Single Electron Turnstile

The system of gates used to implement the single electron turnstile is shown in Fig. 3.10. There is a central 'turnstile' gate V_{tu} with two barrier gates on the left V_{tbl} and right V_{tbr} of it. An entrance and exit gate (V_{en} and V_{ex}), which determine the entrance and exit potentials of the charges and act as reservoirs for the charges before and after being pumped.

As discussed in the theory section on single electron devices in AlGaAs heterostructures (Sec. 2.3.1), the charging energy of the quantum dot used is given by $E_c = \text{e}^2/C_{\Sigma}$ where C_{Σ} is the sum of the capacitances between the dot and its surroundings. The larger this energy, the better the fidelity

of the current (as it reduces the parasitic quantum back-tunnelling current) and the better the control over it.

One of the main benefits of using superfluid helium as the substrate for a single electron device is the lack of screening caused by the film, making the Coulomb potential U_{co} between charges strong. It will thus contribute significantly to the charging energy of the dot above the turnstile gate, making $E_c = \mathrm{e}^2/C_\Sigma + U_{co}$.

The Coulomb potential U_{co} is given by the well known equation

$$U_{co} = \int_0^{r_c} F_{co}\,\mathrm{d}r = \frac{\mathrm{e}^2}{4\pi\epsilon_{\mathrm{He}}}\int_0^{r_c}\frac{1}{r^2}\mathrm{d}r = \frac{\mathrm{e}^2}{4\pi\epsilon_{\mathrm{He}}}\frac{1}{r_c}\,, \tag{3.24}$$

where

r_c is the distance between two charges,

ϵ_{He} is the permittivity of liquid ^{4}He ($9.36 \times 10^{-12}\,\mathrm{F/m}$).

In the case of the device that was fabricated, $r_c = w_{tu} \simeq 0.5\,\mu\mathrm{m}$ (refer to Sec. 3.4.2) making $U_{co} \simeq 2.7\,\mathrm{meV}$.

In order to achieve deterministic single electron transport, a single charge must become trapped in the potential well created above the turnstile gate during each transport cycle. The depth of this well ΔU_w would thus need be greater than the thermal energy of an electron, which at $T = 1\,\mathrm{K}$ $E_{th} = \mathrm{k_B}T \simeq 0.09\,\mathrm{meV}$, but less than the dot's charging E_c. If it is assumed that the charging energy was dominated by the Coulomb potential, then $E_c \simeq U_{co} \simeq 2.7\,\mathrm{meV}$. If $\Delta U_w > E_c$ then more than one charge could be present inside the dot at one time.

After conducting multiple finite element model (FEM) simulations of the device, a sample is shown in Fig. 3.11, it was found the following gates voltages: $V_{en} = V_{ex} = 1\,\mathrm{V}, V_{tbl} = 0.95\,\mathrm{V}, V_{tbr} = 0.9\,\mathrm{V}, V_{tu} = 1.05\,\mathrm{V}$ produced a well depth of $\Delta U_w = 1.3\,\mathrm{meV}$ at the surface, which would successfully isolate a single electron.

Fig. 3.12 shows the sequence of steps involved in clocking a single charge through the turnstile gates.

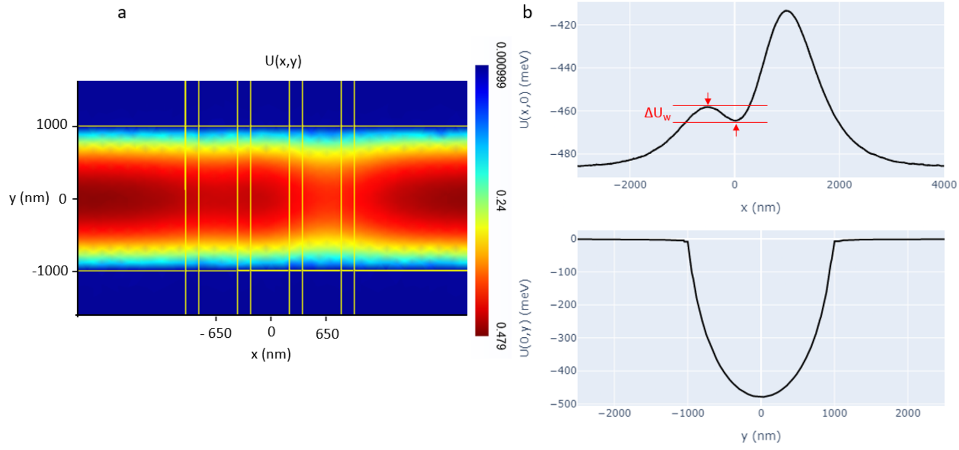


Figure 3.11: **(a)** shows a finite element model (FEM) of the potential at the fluid surface $U(x, y)$ around the turnstile gates, at a moment in time during a pumping cycle (step **(c)** in Fig. 3.12). **(b)** shows the potential plots in the x and y-directions. The quantum dot is at $(0, 0)$. The well-depth of $\Delta U_w = 1.3\,\text{meV}$ is shown in red, along the x-axis. Software used: GMsh

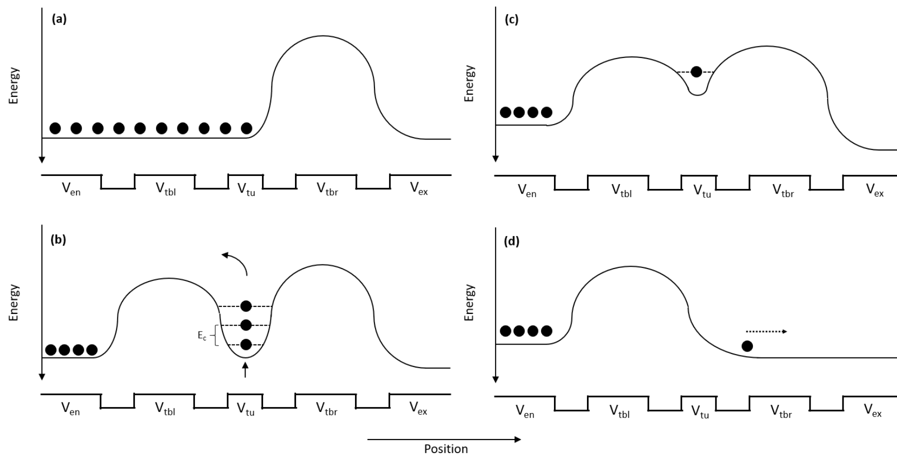


Figure 3.12: An example of the potential energy profile at the fluid surface above the turnstile gates for a single transport cycle. Step **a** shows the loading of the turnstile dot by lowering the left barrier potential. Step **b** shows the 'back bleeding' that makes the dot smaller, removing all but one charge from the dot. Step **c** shows the one charge that is left and step **d** shows the unloading of the dot by lowering the right barrier potential and the charge moving away.

3.3 Requirements

The design and fabrication requirements needed to ensure the device's successful operation and optimal performance are detailed in this section.

3.3.1 Bottom Gates

- The conductivity of the metal used should be high to reduce resistive losses in the measured and applied signals.

- The grain density of the metal should be reduced as much as possible. Grains lead to work function variations in the metal's surface, which affect the electric potential produced by the gate at the fluid's surface.

- The surface roughness of the gate should be kept as low as possible, as it is related to the grain density [51].

- The gap width between gates w_g should be made as small as possible to reduce the barrier potential the charges must overcome to get to the next gate. This would allow for smaller voltage amplitudes to be used to transfer the charges, which in turn reduces scattering.

- The variations w_g should be reduced as much as possible, as too great a variation would cause different amounts of charge to be transferred between gates per channel.

3.3.2 Top Metal

The top metal has the same material requirements as the bottom gates, specified above.

3.3.3 Channels

- The channel width should be made as small as possible to maximise the critical charge density $n_{s,c}$ (from Eq. 2.27) and to fit as many channels as possible into the central part of the device.

- The channel height should be low enough to maximise $n_{s,max}$ (from Eq. 3.6) (with $V_r = 0.5\,\text{V}$) without breaking the requirement below, but tall enough to keep the minimum depth d_o (from Eq. 2.29) of the fluid in the channel greater than 90% of the channel's height (when $n_s = n_{s,max}$).

- The maximum charge density $n_{s,max}$ should not be close to the critical charge density $n_{s,c}$.

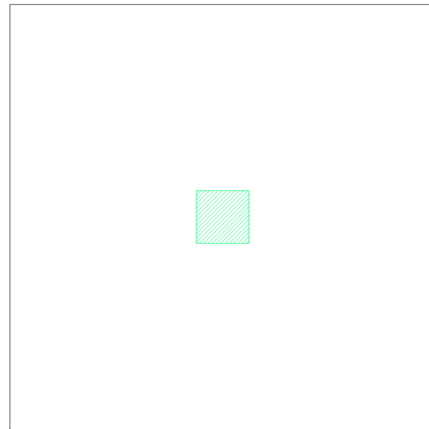
- A material with a low dielectric constant should be used to reduce the coupling between the top metal and the bottom gates. This, in turn, will improve the SNR of the sense signal by improving the coupling to the HEMT's input gate over the surroundings and by reducing the total capacitance of the system (refer to Eq. 3.4).

3.4 Design and Fabrication Process

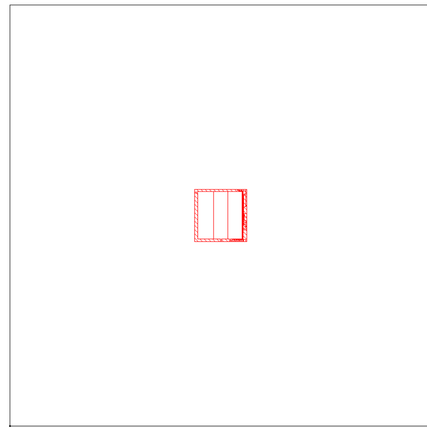
In this section, the design of the six lithography layers that define the device geometry, shown together in Fig. 3.4, and the process developed to fabricate the design are presented. The design and fabrication choices made for each layer are detailed and are related back to the requirements specified in Sec. 3.3. Fig. 3.2 shows an overview of the device.

3.4.1 Wafer Selection

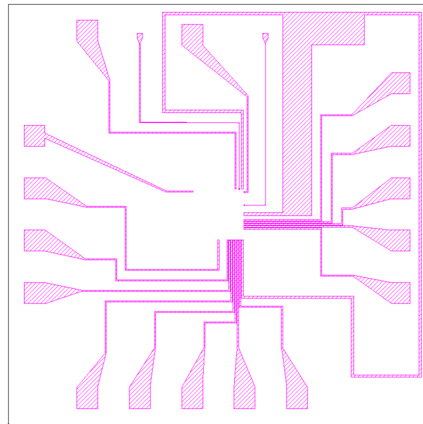
A standard 4-inch silicon wafer with a high quality, thermally grown 3.5 µm layer of SiO_2 was used as the base substrate for the device fabrication. The oxide layer was needed to ensure that the device is well isolated from spurious signals that may be present on the PCB to which it is mounted.



(a) M1 - Bottom Metal Square (deposition)

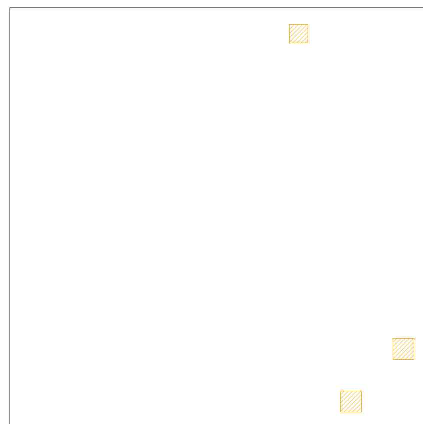


(b) M2 - Bottom Gates (etch)

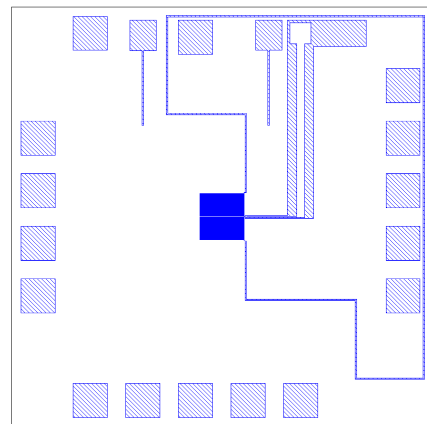


(c) M3 - Bond Pads and Traces (deposition)

(d) M4 - Top Metal Square (deposition)



(e) M5 - Top Thickenning (deposition)



(f) M6 - Channels and Top Gates (etch)

Figure 3.13: The six lithography process layers that define the geometry and function of the device. A close up of the gates in layers **(b)** and **(f)** are shown in Fig. 3.5 and Fig. 3.4.

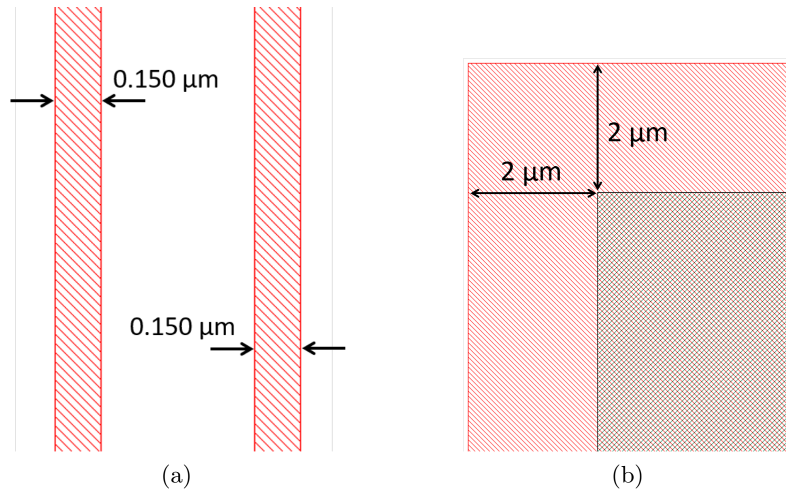


Figure 3.14: **(a)** Gate 150 nm gap width size. **(b)** Overlap tolerance of 2 µm between the M1 deposition and M2 etch layers.

3.4.2 Bottom Gates

The fabrication of the bottom gates was designed as a two step process involving, first, an optically patterned layer of squares (see Fig. 3.13 **(a)**) for the deposition of the gate metal followed by an Electron Beam Lithography (EBL) defined etching layer (see Fig. 3.13 **(b)**).

The use of an EBL was necessary to achieve the smallest possible gap sizes between the gates. After some experimentation, a designed $w_g = 0.15\,\mu\text{m}$ gap size was chosen, shown in Fig. 3.14 **(a)**. The write-field of the EBL machine was limited to $1\,\text{mm}^2$ and constrained the geometry of the gates, as the design avoided stitching (needing to move the EBL stage). The second layer had to completely cover the first as it defines an etch. The tolerance for this overlap is shown in Fig. 3.14 **(b)**.

Additionally, a two-step (deposition/etch) approach was taken because writing the mask for a direct deposition would lead to excess scattering of the electron beam caused by the thick insulating oxide layer present on the wafer beneath the resist charging up and, given its thickness, making it impossible to drain from the backside of the wafer. This charging would have contributed to gap width variations, which needed to be avoided as per the requirements (refer to Sec. 3.3.1). The metal plate, although isolated, provided some drain for the charges. However, charging did remain a problem throughout as the plate was quite small. This process is shown in Fig. 3.15.

SPR 955 on top of LOR 3A were the chosen optical resists, both positive. LOR develops at a higher rate than the SPR using CD-26 creating some undercut that mitigates against sharp spurs forming along the edge of the deposited metal.

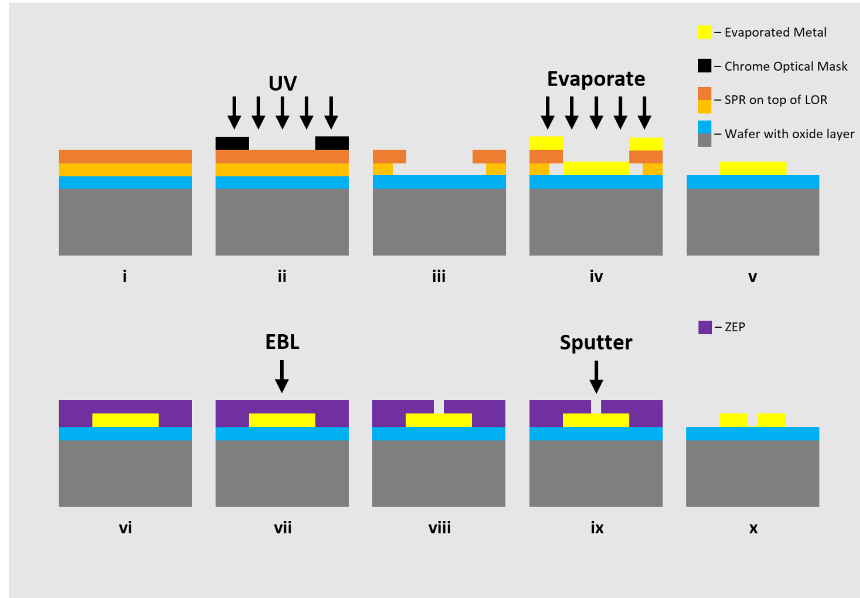


Figure 3.15: Process of defining the bottom gates, involving first an optically defined metallisation and lift-off process (top row), followed by an EBL defined sputter etch (bottom row).

Electron-beam physical vapour deposition (EBPVD), or just E-Beam Evaporation, was the chosen thin film deposition method for the metal layers. E-Beam Evaporation involves firing a high powered electron beam at a metal target under high vacuum, causing the metal to sublimate. The wafer is placed within 'line-of-sight' of the sublimated metal atoms, which condense onto it and coat it. The rate of the deposition is measured and can be controlled by varying the power of the beam. An advantage to the condensation process of E-Beam Evaporation is that a low deposition rate can be achieved, which produces a film with low grain density, as specified in the requirements (Sec. 3.3.1). A deposition rate of between $0.01\,\mathrm{nm\,s^{-1}}$ to $0.05\,\mathrm{nm\,s^{-1}}$ was chosen.

A thickness of 27 nm was chosen for the bottom gates, from a combined stack of 5 nm Chromium (Cr), 20 nm Gold (Au), 3 nm Cr. The thin Cr layers are needed as they act as an adhesive between the Au layer and the various oxides surrounding it. Au, being a noble metal, does not form strong bonds with oxides but does alloy well with other metals. Cr, on the other hand, does form strong oxide bonds. A vacuum must be kept through the deposition process to prevent the Cr from oxidising.

An argon plasma sputter etch was the chosen method to etch through the metal to define the gates. Argon sputter etching is a common metal etching process that involves directing an argon plasma towards a target to cut through it. Argon is used as it is highly unreactive. An etch time of 30 s

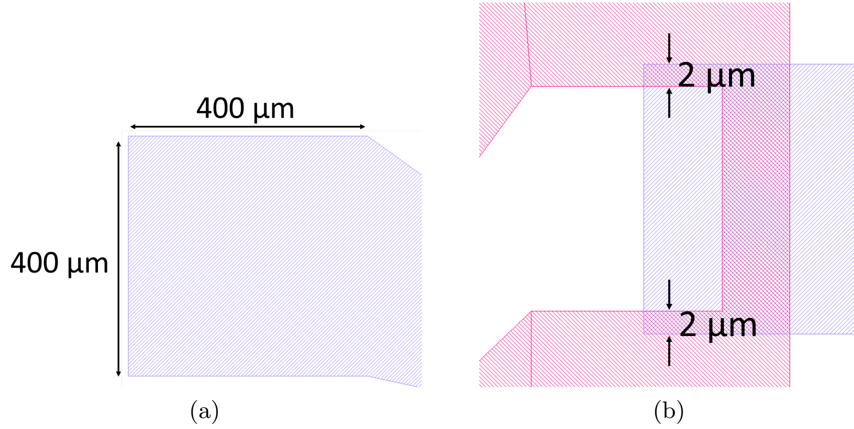


Figure 3.16: **(a)** 400 µm × 400 µm bond pad size. **(b)** Overlap tolerance of 2 µm between the M2 and M3 layers, also showing how the traces in M3 connect to the gates in M2.

was found to be sufficient to etch through the thin 27 nm metal layer.

An important design choice made was the width of the turnstile gates chosen to be $w_{tu} = 0.5\,\mu\text{m}$ and the width of barrier gates on the either side of it chosen to be $w_{tb} = 1\,\mu\text{m}$. This made $U_c \approxeq 2.7\,\text{meV}$ (refer to Eq. 3.24).

3.4.3 Bond Pads and Traces

The bond pads and traces layer (Fig. 3.13 **(c)**) shows the bond pads as squares along the edges, with the traces connecting them to the bottom gates. A maximum of 6 bond pads per side was allowed by the design of the electronics and the pin capacity of the connectors chosen.

The surface area of the bond pads was made large to improve the chances of a successful wire bond, chosen to be a 400 µm by 400 µm square as shown in Fig. 3.16 **(a)**. Fig. 3.16 **(b)** shows the ±2 µm overlap tolerance between the traces and the tabs on the bottom gates, which was sufficient given the use of sub-micron accuracy vernier marks for optical alignment (shown in Fig. 3.21).

A 50 nm layer of Au deposited by E-Beam Evaporation was the chosen layer thickness and deposition method for this layer. An adhesive Cr layer was not needed as the size of the patterning was sufficient to adhere to the oxide substrate beneath.

A very short sputter etch was performed before the deposition to remove oxidised Cr on the bottom gate tabs, minimising the formation of tunnel junctions between the two layers.

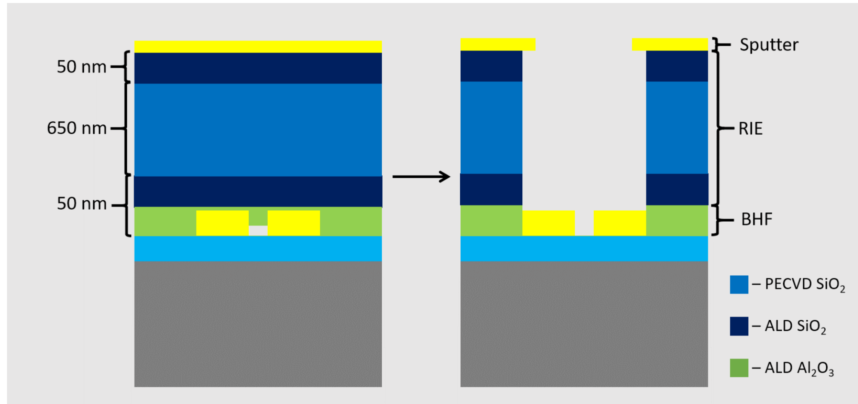


Figure 3.17: *Left:* Device oxide mid-section with top metal. *Right:* Final top gate and channel forming etch process.

3.4.4 Channels and Top Metal

After the bottom metal layers, the oxide layers that make up the mid-section of the device (i.e. the channel walls) were deposited. This was followed by an optically patterned layer of simple squares for the top metal deposition (Fig. 3.13 **(d)**) and then by patterning a thickening layer (Fig. 3.13 **(e)**), to thicken areas of the top metal that would be wire bonded to.

The final layer (Fig. 3.13 **(f)**) is an optically patterned etching layer that defines the channel geometry and the top metal gates, and opens up 'windows' through the oxide layers to the bottom metal bond pads.

The width and height of the channels were important design parameters, as detailed in the requirement for the channels (Sec. 3.3.3). The widths were chosen to be 4 µm with a taper to 2 µm along the sensing region. This improved surface charging by providing more area in which to collect charges while the taper narrowed the channels increasing the charging energy of the area above the turnstile. A width of 2 µm was the minimum achievable using optical lithography.

The height was chosen to be 0.75 µm. This made the estimated critical charge density $n_{s,c} = 3.28 \times 10^{12}$ (Eq. 2.27) and the expected maximum charge density $n_{s,max} = 19.5 \times 10^{12}$ (Eq. 3.6 with $V_r = 0.5\,\mathrm{V}$), which is significantly less than the critical amount ($n_{s,max} \ll n_{s,c}$) satisfying the requirement (Sec. 3.3.3). The minimum depth of the fluid d_o in the channel was estimated at $d_o = 0.74\,\mu\mathrm{m}$ (Eq. 2.29 using $n_s = n_{s,max}$), making the minimum fluid depth 98% of the channel height, which satisfied the requirements (refer to Sec. 3.3.3).

The channel walls were fabricated by the deposition of oxides in three stages. Fig. 3.17 shows the layers and their thicknesses. The first was an Atomic Layer Deposition (ALD) of 20 nm of Al_2O_3 followed by 30 nm of SiO_2. The ALD process deposits a very dense, high-quality conformal

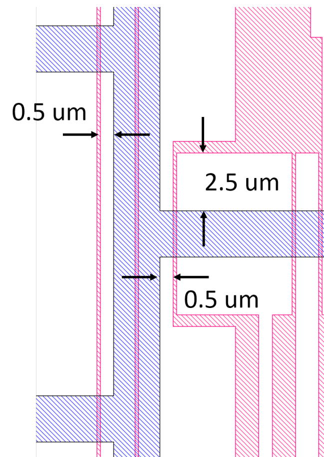


Figure 3.18: The alignment tolerances between the channels and the bottom gates.

coating (atomic layer by atomic layer). It reduces the chance of pin-holes forming (potentially causing shorts between the top and bottom metals) and charge traps forming by mitigating against dangling bonds in the oxide, which introduce noise into the charge sensing signals. The Al_2O_3 layer was used as a stopping layer for the channel etch process as it is more resistant to the Buffer Hydrofluoric Acid (BHF) etchant than SiO_2 (detailed below). This was followed by 650 nm of SiO_2 using a Plasma-Enhanced Chemical Vapour Deposition (PECVD) process. This produces a less dense film compared to the ALD process but does so far quicker. A final layer of ALD 50 nm SiO_2 was deposited, again to prevent charge traps forming close to the liquid surface.

The top metal was a stack of 5 nm of Cr followed by 10 nm of Au, deposited using the usual E-Beam Evaporation process. The top layer was kept thin as it reduced the amount of sputtering needed to get through it.

Three steps were involved in the final channels etch, shown in Fig. 3.17 on the right. The first was a short sputter etch to get through the top metal layer. The second was a Reactive Ion Etching (RIE) process (a dry etch that removes the oxides using a chemically active plasma) used to get through most of the oxide layers. This etching process had to be stopped before reaching the bottom gates, as it could roughen the surface. This was too difficult to do reliably, thus the need for the Al_2O_3 stopping layer and a final BHF 50:1 wet chemistry etch to remove it. BHF is a poor Cr etchant which reduced the risk of surface roughening. Some undercutting of the oxide was expected and, in the case of this device, considered beneficial by reducing the impact of surface charges along the channel walls on the potential at the fluid's surface.

The alignment between the bottom gates and the channels was critical

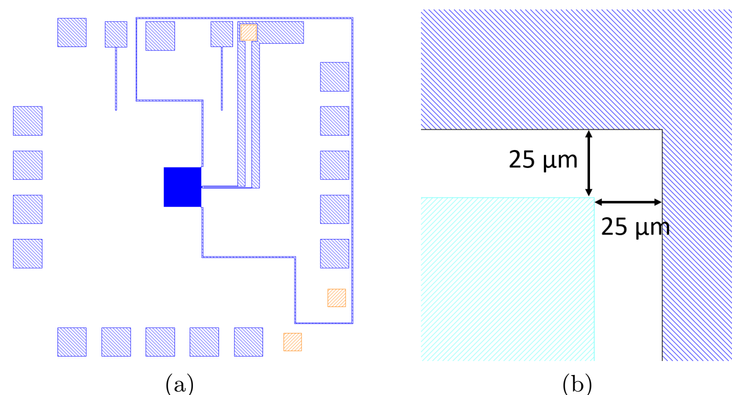


Figure 3.19: **(a)** The thickened areas of the top gates. **(b)** Alignment tolerances between the M5 and M6 layers.

to the correct functioning of the device and was difficult to achieve given the complexity of the final etch steps. Therefore, a tolerance of ±0.5 µm in the x-direction and ±2.5 µm y-direction were built into the design, as shown in Fig. 3.18.

To further mitigate against misalignment, some devices had the top layer purposefully shifted by + or - 0.5 µm in the x-direction relative to the bottom gates. This meant if there was a significant alignment problem in the x-direction, some devices may still yield successfully.

Fig. 3.19 **(a)** shows the thickening layer (Fig. 3.13 **(e)**) overlayed on the channels layer. These were regions of the top metal that were to be wire bonded to and had to be thickened, as the 15 nm thickness of it made the possibility of lifting the thin metal layer off during bonding a concern.

3.4.5 Global Layout and Alignment Marks

The device design was repeated and spread to fill the space available on the 4-inch wafer, shown in Fig. 3.20, with a yield of 55 devices in total.

Optical alignment marks are present on the right and left sides of the wafer. These vernier marks, shown in Fig. 3.21, provide sub-micron accuracy when used.

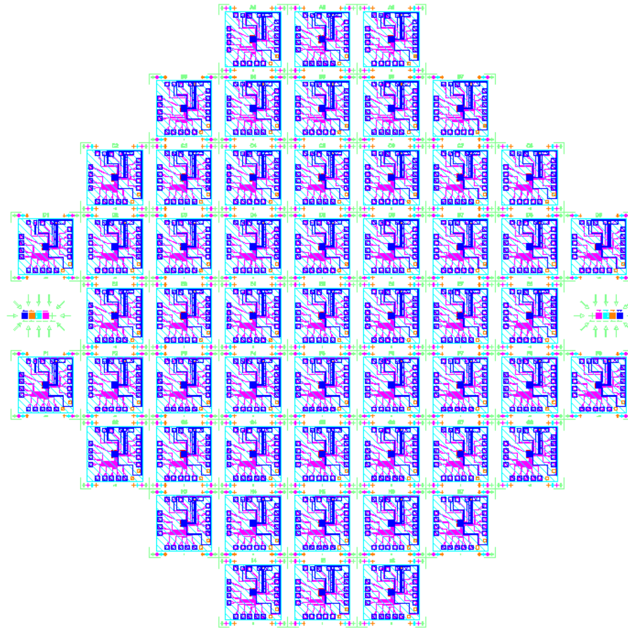
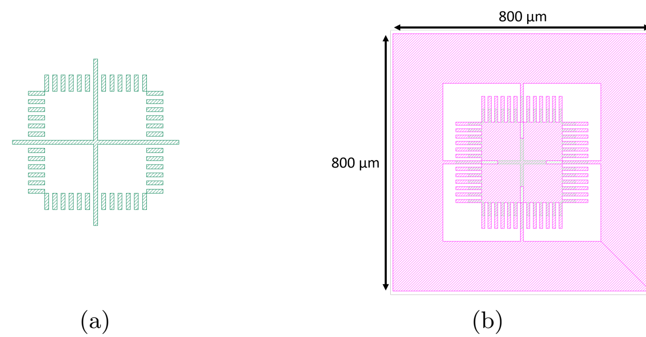


Figure 3.20: The layout of the devices on the wafer, with a total yield of 55 devices fitting into the 4-inch wafer.



(a) (b)

Figure 3.21: **(a)** The alignment pattern deposited on the first layer. **(b)** The vernier mark used to align to the deposited mark underneath.

3.5 Process Development

The development of the fabrication process involved defining the steps and determining the parameters needed to fully and successfully fabricate the device. The output of this was the fabrication procedure given in App. A.

Some of the work that went into producing this process is presented in this section.

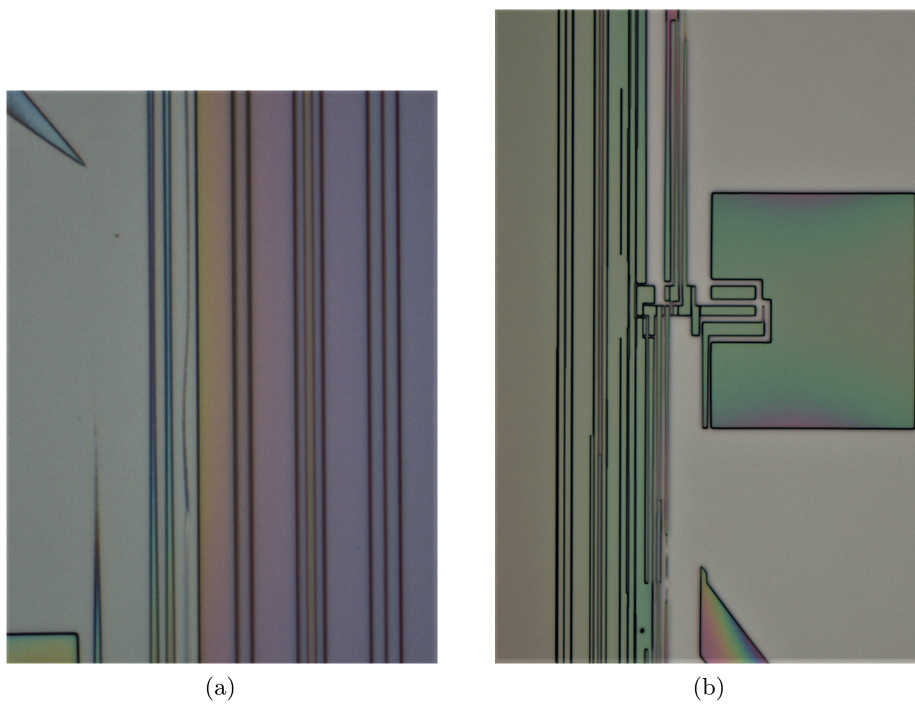
3.5.1 EBL Etch Mask

The etch mask for the bottom gates was written using EBL and the correct exposure dose had to be determined. Beam scattering was a concern given the charging effects of the relatively small metal square, isolated above the thick oxide layer, that the mask was patterned over. An algorithm called Proximity Effect Correction (PEC) was applied to the mask design to correct for the effect of primary electron scattering, which tends to increase and uncontrollably vary the feature size being patterned. PEC takes into account the materials underlying the resist (27 nm metal on top of 3.5 µm of SiO_2) and outputs an array of regions that vary the beam's base intensity. It can also improve the fidelity of smaller features that require higher exposure.

Finding the right base dose was crucial as underexposure leads to poor mask development and problems when etching, while overexposure degrades the mask (as shown in Fig. 3.22 **(a)**) and can warp features. A higher dose is better for smaller features, however. Base dose tests ranging from 450 µC/cm^2 to 650 µC/cm^2 were performed with 500 µC/cm^2 found to be optimal. An issue with the CAD file was found after a week of it causing problems: the lines in the file were doubled causing massive artefacts to develop in the mask, shown in Fig. 3.22 **(b)**.

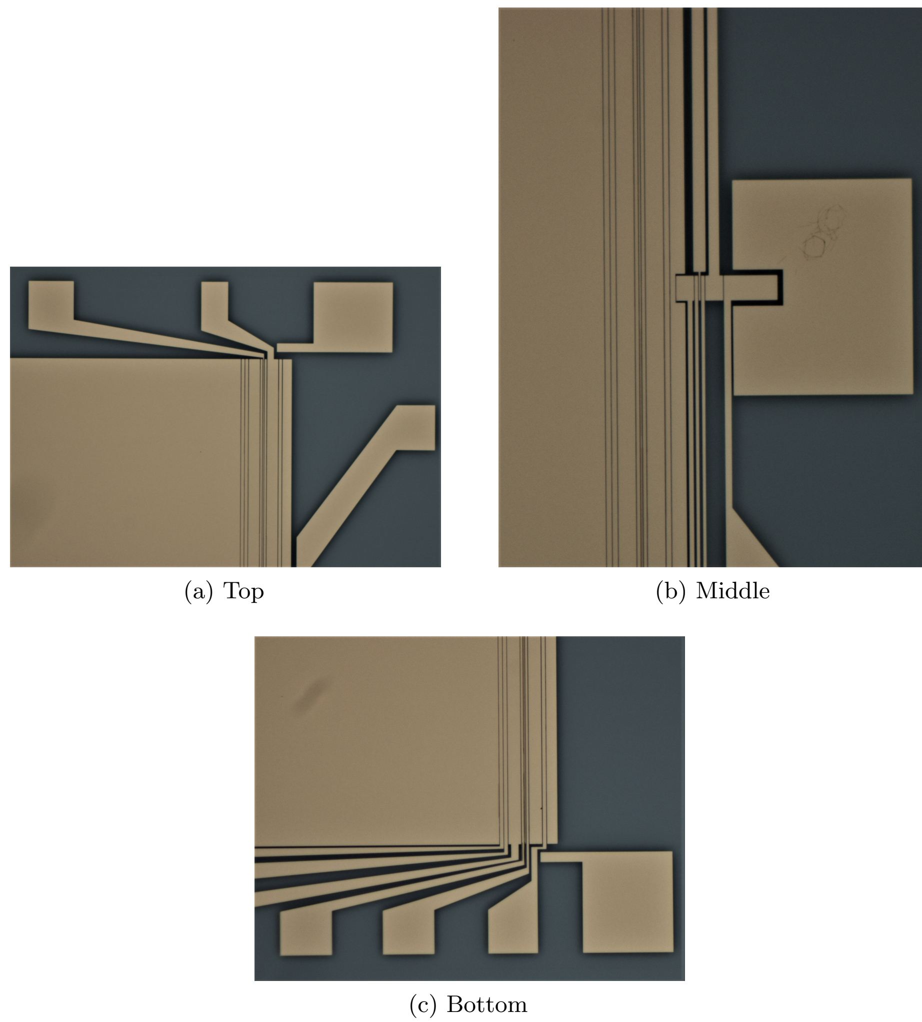
The images in Fig. 3.23 show the etched gates after the correct dose was found and problems with the design were sorted out. A sputter etch timing of 30 s was found to work after a few trial runs were performed.

Upon closer inspection of the gates using a Scanning Electron Microscope (SEM), a problem was found. The gap widths between the long parallel channels gates were found to be greater at the top of the gates compared to their midsections, as shown in Fig. 3.24. A possible solution is to split the EBL step into two. First, the larger parts would be exposed and etched followed by exposing and etching the much smaller gaps between the gates. This would, however, increase the processing time and complexity. At the time of writing, no solution has been tested due to the COVID-19 pandemic and global lockdowns.



(a) (b)

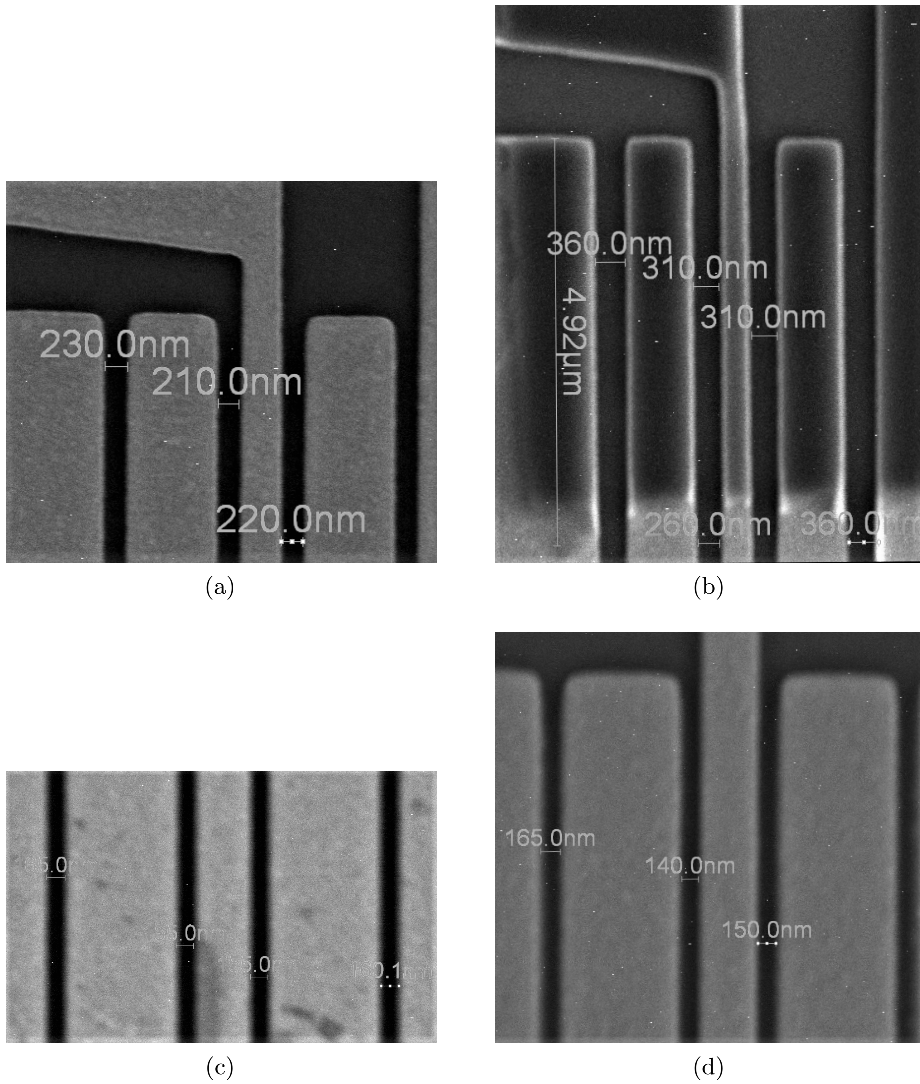
Figure 3.22: **(a)** The effect of overexposure with some of the mask being completely developed away. **(b)** Artefacts caused by the doubling up of the lines in the EBL CAD file.



(a) Top (b) Middle

(c) Bottom

Figure 3.23: Bottom gates after etching. Refer to Fig. 3.5 for the design.



(a) (b)

(c) (d)

Figure 3.24: The SEM images in **(a)** and **(b)** are of the top sections of the bottom gates, showing measurements of the gap widths between the gates. These differ significantly from the designed values of 150 nm. The base dose intensity in **(a)** was 500 µC/cm^2 while in **(b)** is was 650 µC/cm^2, which demonstrates the observed trend: the increase in the variation with an increase in the base dose intensity. The SEM image **(c)** shows the gaps at the mid-sections of the gates and in **(d)** the gaps between the experimental channel gates, both were around 160 nm which was within the tolerance range.

3.5.2 Alignment

The optical alignment between photolithography layers was very good as seen in Fig. 3.25. However, the alignment between the channels and the bottom gates was greater than the allowable tolerances, with an error of approximately 0.5 µm in the x and 2.5 µm in the y (shown in Fig. 3.30 **(c)**). This suggests that there was something wrong with the EBL machine aligning to the chip-level markers. Additional full fabrication runs are needed to fully diagnose the problem, as it may have been a once-off error.

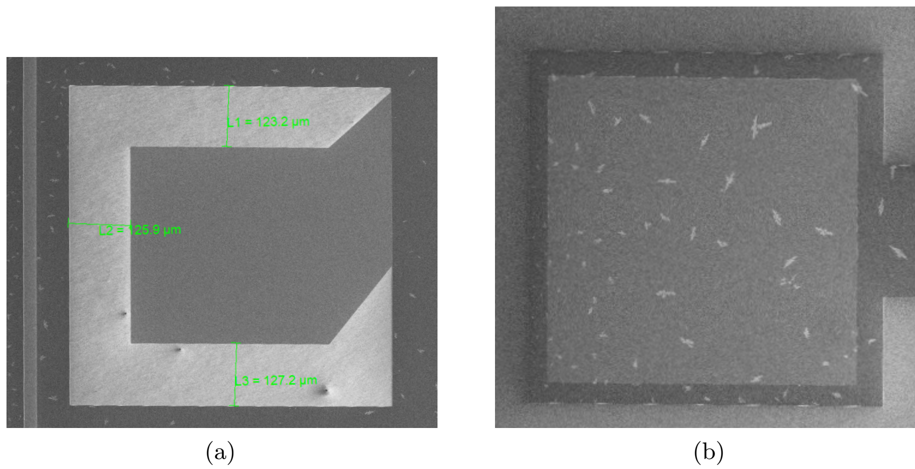
3.5.3 Channels

The deposition and etch rates for the channel oxide layers had to be determined. Various tests (around 17 in total) were conducted, the results of which are shown in Fig. 3.27 and Fig. 3.28. These tests verified both the deposition and etch rates, as the thickness of the oxide layer had to be measured after each deposition and after each etch. These film thickness measurements were done using reflectometry, which uses the refractive index of light shone onto a spot to estimate the height of the various materials on the wafer by fitting a model to it, Fig. 3.26 shows an example.

Each test was conducted by first preparing a wafer with an oxide substrate of interest, measuring the thickness of film and then etching it for a set amount of time, using an etching method of interest. After each etch, the height would be remeasured and recorded and so on. Linear functions fitted to the data gave the etch rate. These rates were generally consistent between etches and were found to be consistent when compared to previous data the lab had.

The full-stack etch (sputter, RIE, BHF 50:1) proved to be successful, Fig. 3.29 shows how the channels looked afterwards. However, some concern was raised over the profile of the channel walls and the pot-marked edge of the top metal (shown in Fig. 3.30), which could cause excessive local field concentrations around it or otherwise unwanted potential variations at the fluid's surface. These could lead to the field emission of charges into the channels or other dielectric breakdown phenomena and possibly ruin the device's ability to achieve quantised single electron transport. The only way to determine whether this effect will be significant is to test it and at the time of writing, no device has been successfully fabricated.

If found to be too problematic, a possible mitigation strategy could be to use a hard etch mask that would straighten the edge of the top metal by reducing the roughening caused by the metal sputter etch. This straight edge would then lessen the ridges seen in the channel wall profile by shielding it from the RIE etch.



(a) (b)

Figure 3.25: Examples of the acceptable optical alignment.

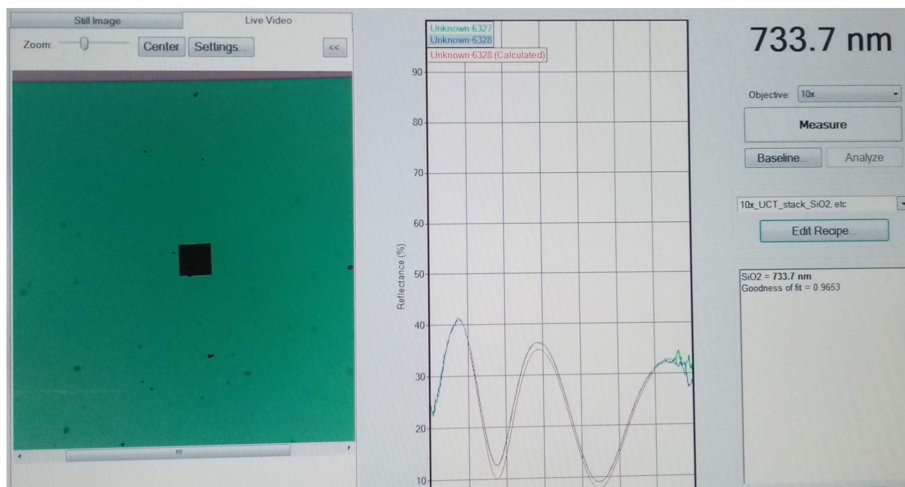


Figure 3.26: Reflectometry measurement example, measuring the height of the oxide stack used for the channels.

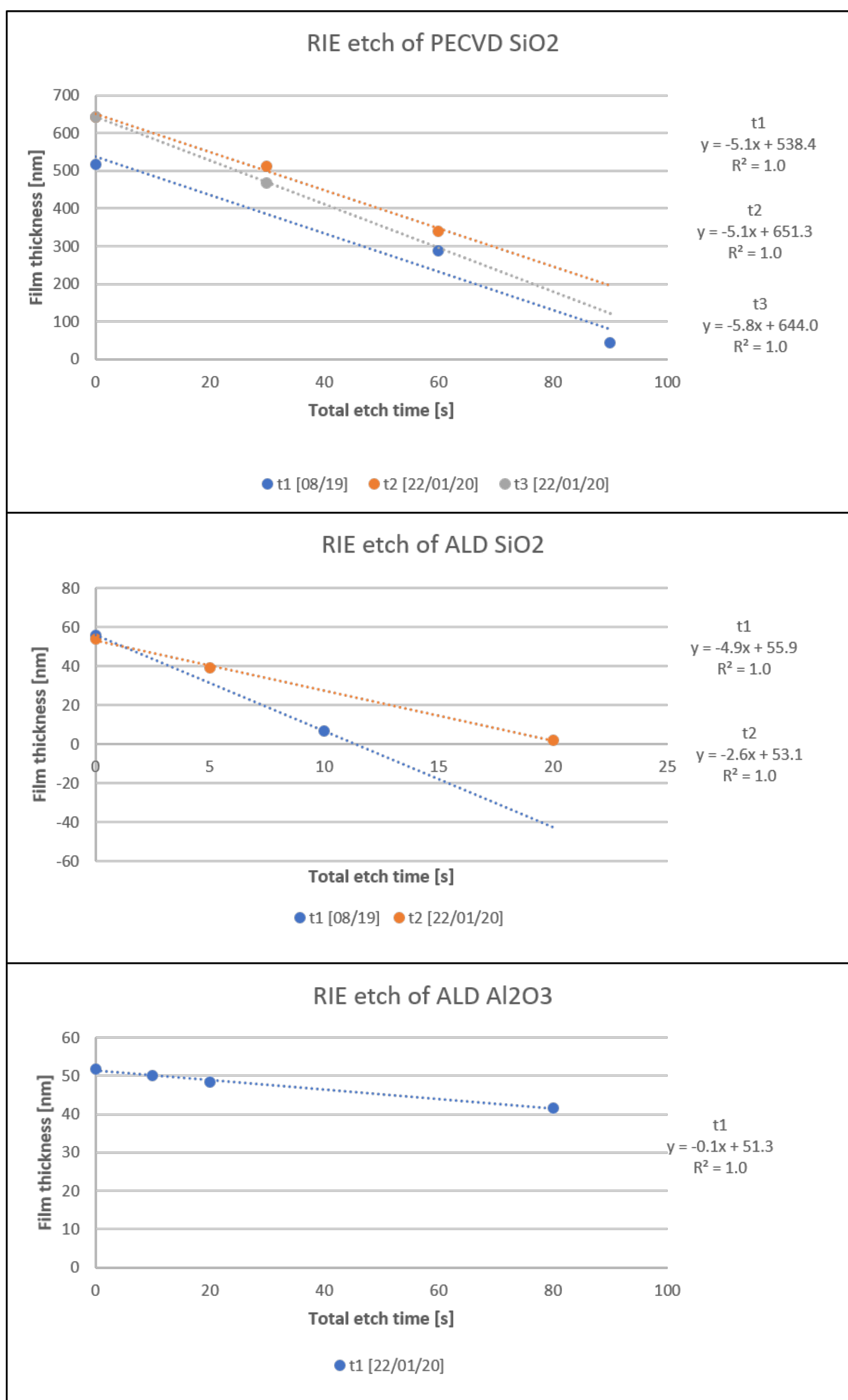


Figure 3.27: Data from the RIE etch rate tests for all three oxide materials used.

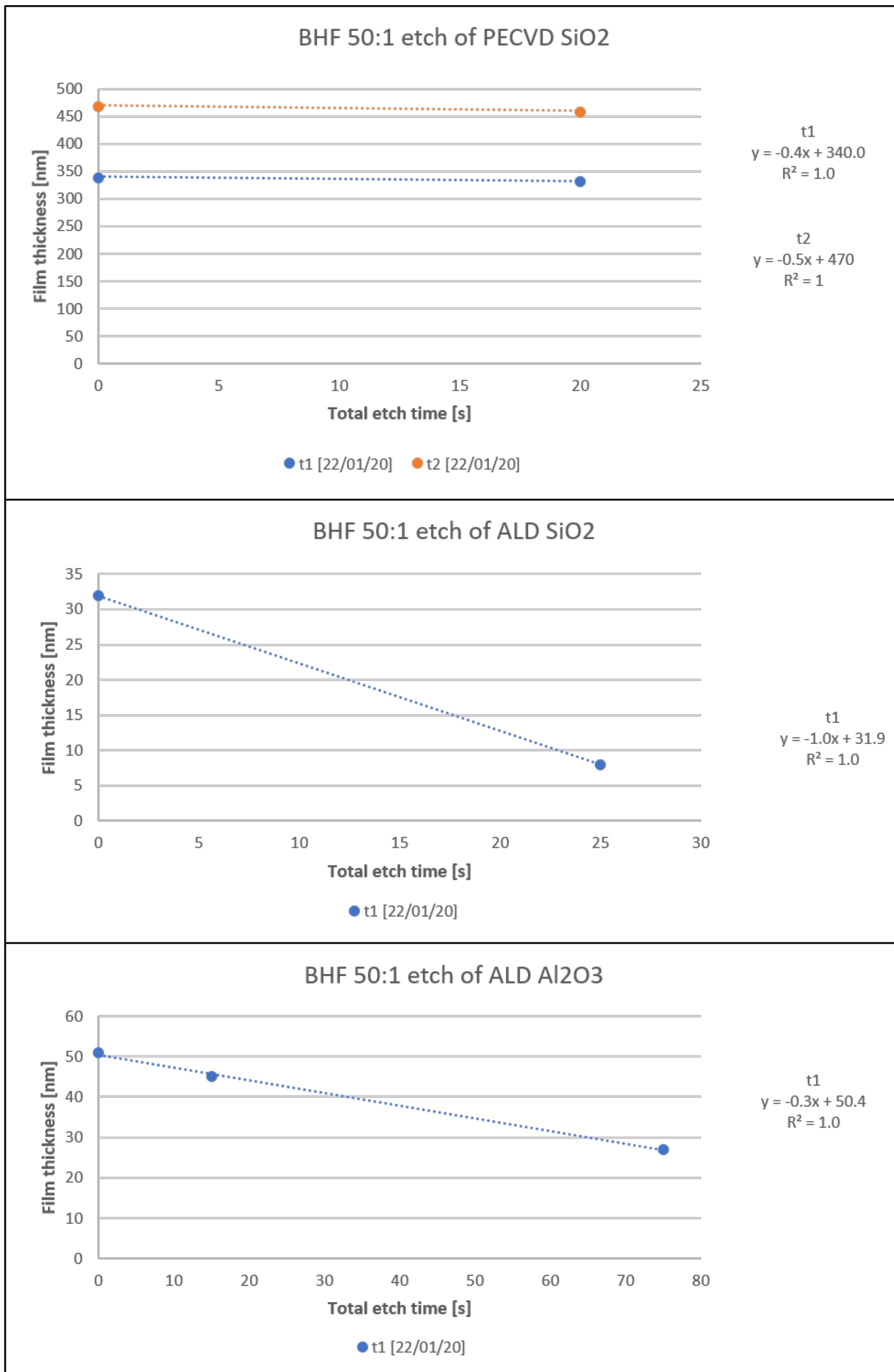
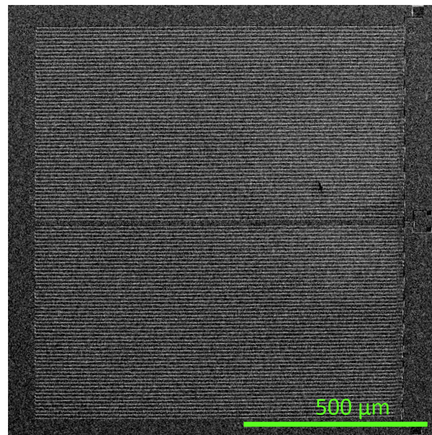
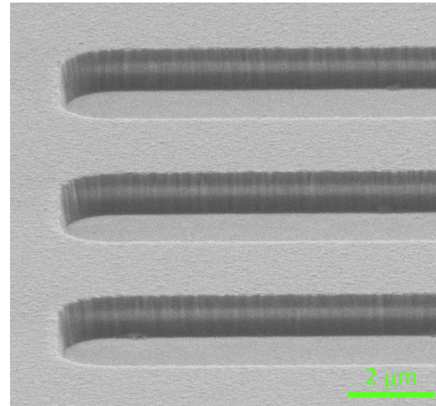


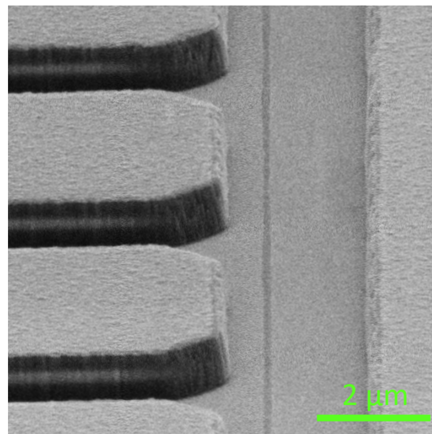
Figure 3.28: Data from the BHF 50:1 etch rate tests for all three oxide materials used.



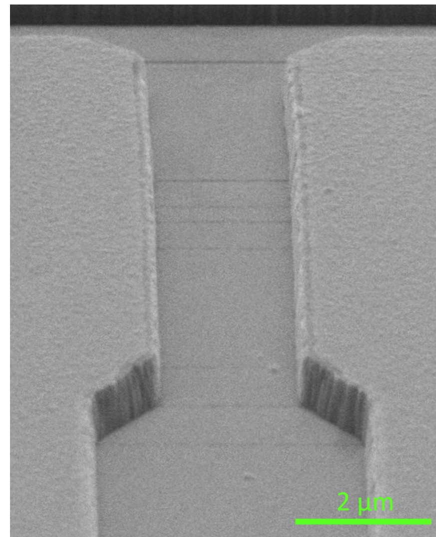
(a) Overview of the 120 channels



(b) Channel beginngings

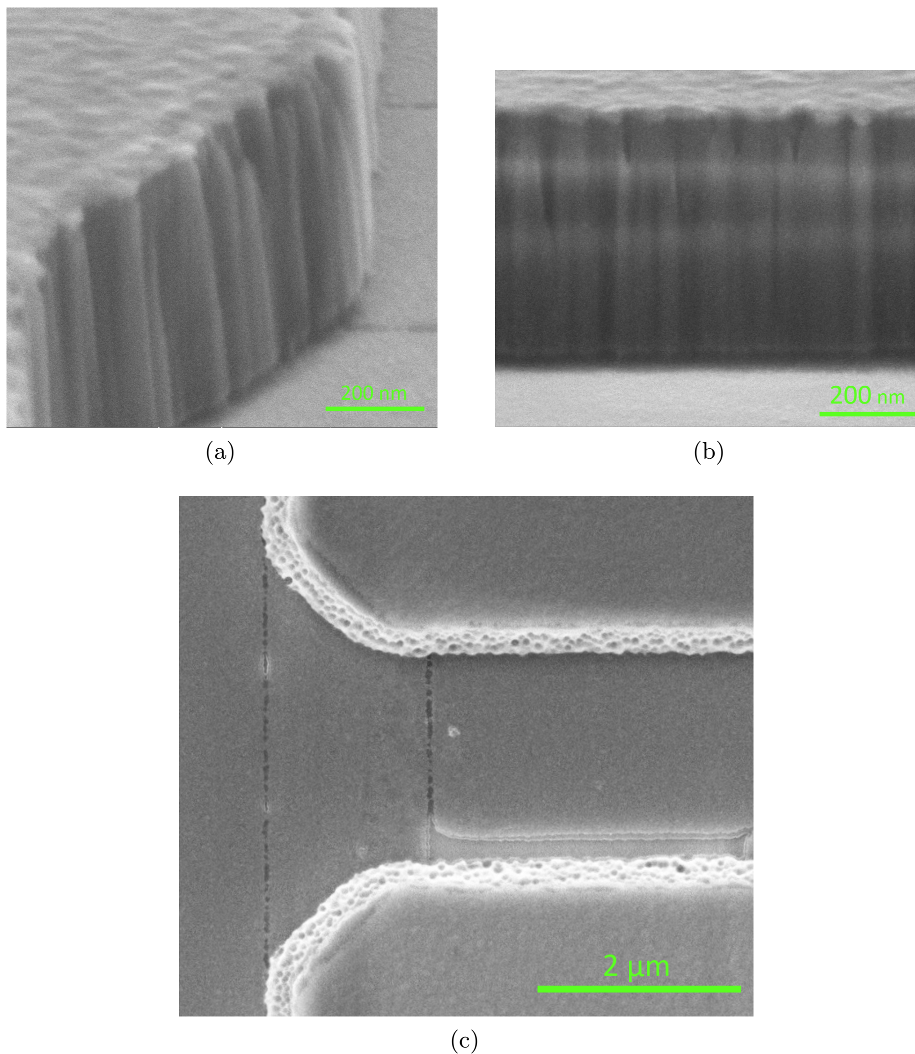


(c) Channel ends



(d) Angled view of channel ends

Figure 3.29: SEM images of the etched 2 µm wide channels of device. The metal for the top and bottom gates can be seen in light grey, with the oxide of channel walls in darker grey.



(a) (b) (c)

Figure 3.30: SEM images of various parts of the device. **(a)** Close-up of an angled channel side wall. **(b)** Close-up of a straight side wall. **(c)** The edge of the the metal at the top of channels, with pot-marks from sputter etching. Also shown is the misalignment between the channels and the bottom gates.

CHAPTER 4

ELECTRONICS

4.1 Overview

Electronics defined on Printed Circuit Boards (PCBs) were needed to control and read signals from the device's gates, which would be wire bonded to the PCBs. These boards had to fit inside of a hermetically sealed cell (see Sec. 5.1) which was lowered into place in the dilution fridge using a probe. The dimensions and layout of the boards were thus constrained by the cell's design. Additionally, the components used on the PCBs (and the PCBs themselves) had to be able to function at the extremely low temperatures present inside the cell.

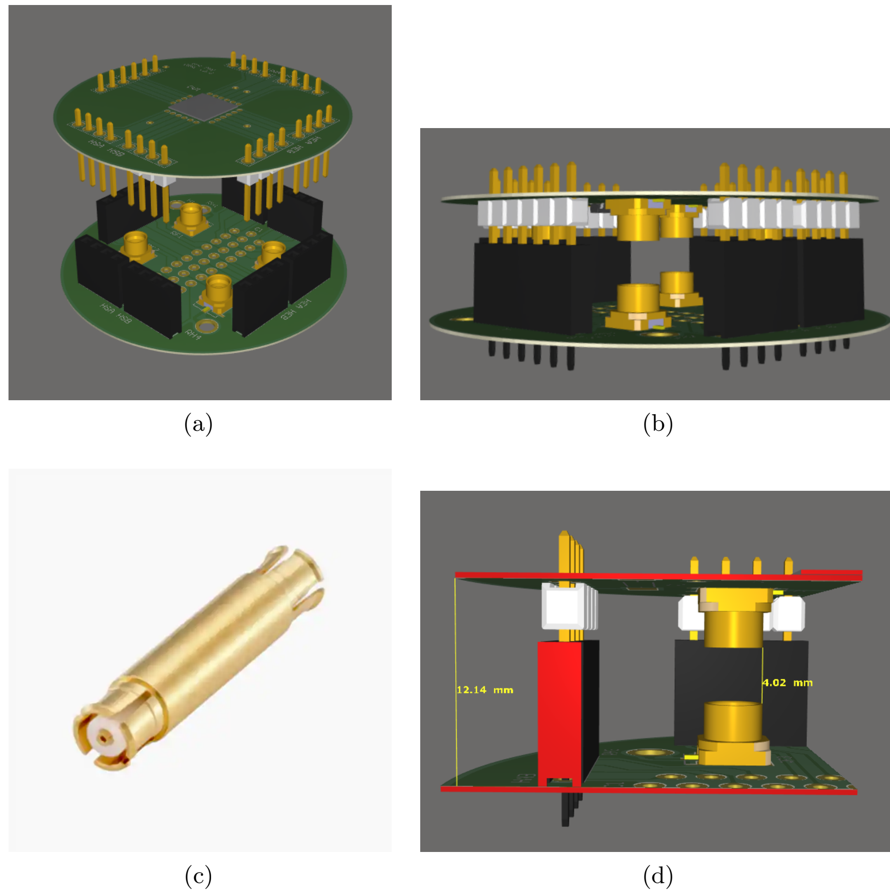
There were two primary PCBs, one stacked on top of another (as shown in Fig. 4.1). The bottom board, called the Motherboard (MBD), interfaced with the connectors present in the cell (a 31-pin connector for bias voltages and four co-axial pins for sensitive, oscillatory signals). Connecting into it from above was the Device Holding Board (DHB), that was wire bonded to the fabricated device.

Given the space constraints present inside the cell, this two-level approach was chosen as it was more compact and it allowed for some flexibility in the design of different DHBs for different device gate layouts.

The diagram presented in Fig. 4.2 shows an overview of the system as a whole, showing the inputs and outputs for each sub-system and the connections between them. From this abstract viewpoint, the device has inputs for bias voltages and two RF signals, for the two twiddle gates, and two outputs for the RF signals from the sense gates. The signals from the sense gates are the only way to gather any data from the device. As can be seen from the diagram, these output RF signals are first amplified by a Cascode amplifier before being fed back into the compare channel of a

lock-in amplifier. The lock-in amplifier takes a reference signal from the signal generator outputting the signals for the twiddle gates. By doing this, the lock-in is able to tune into the exact frequency being used, mitigating against noise, and finally outputting the magnitude of the change in the potential induced on the sense gates, which is used to determine the number of electrons being sensed (refer to Sec. 3.2).

I was primarily responsible for designing the PCBs, sourcing the needed components and testing the boards once made. The PCBs were designed using Altium Designer and were fabricated by Trax Interconnect (Pty.) Ltd. in Cape Town. Some testing prototype boards were CNC'd in-house at UCT. Although the final designs presented are simple, a lot of time was spent on the layout of these boards given the tight constraints and the design of the superfluid device changed several times.



(a) (b) (c) (d)

Figure 4.1: Renders of the top Device Holding Board connecting into the bottom Motherboard are shown in **(a)** and **(b)**. The Rosenberg 19K104-K00L5 ‘Bullet’ connector is shown in **(c)**, used as the interconnect between the RF ports on each board. A render of a slice through each board is shown in **(d)**, with a measurement of the spacing between the boards and the RF ports. A gap of 4 mm is small enough for the bullet connector shown in **(c)** to fit.

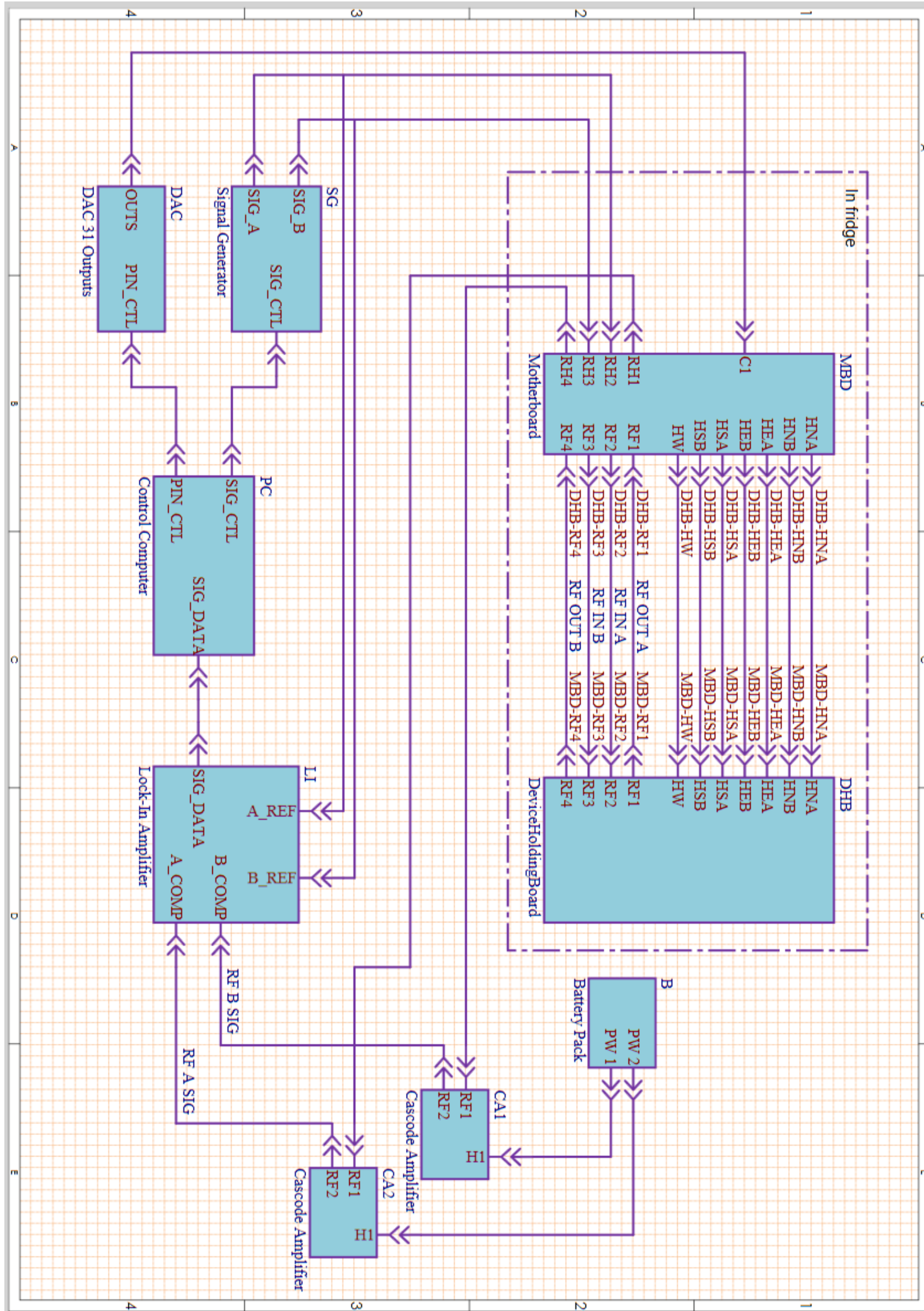
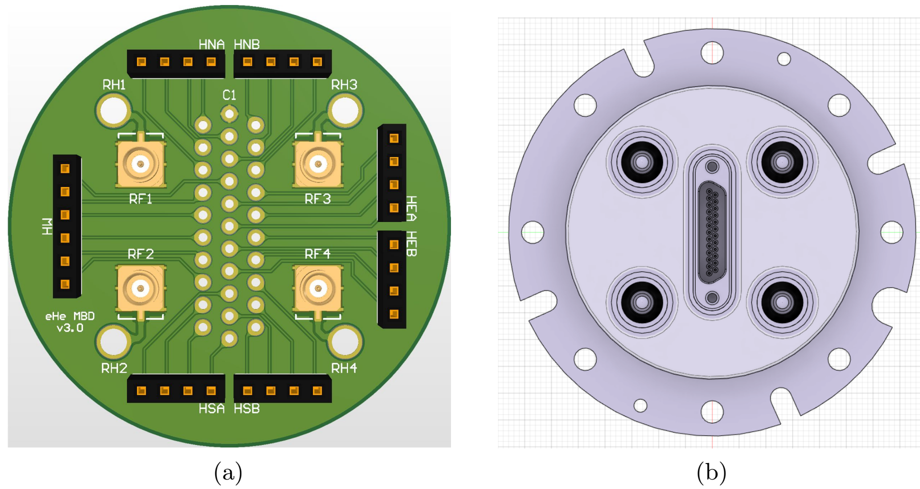


Figure 4.2: The system overview showing the various subsystems and the connections between them.

4.2 Motherboard

As previously stated, the Motherboard (shown in Fig.4.3 **(a)**) was designed to interface with the connectors present in the cell (shown in Fig.4.3 **(b)**). This comprised of a Male Micro-D type 31-pin connector (interface MIL-DTL-83513/2) needed for the various bias voltages. There were another four co-axial pins for the charge sensing signals.

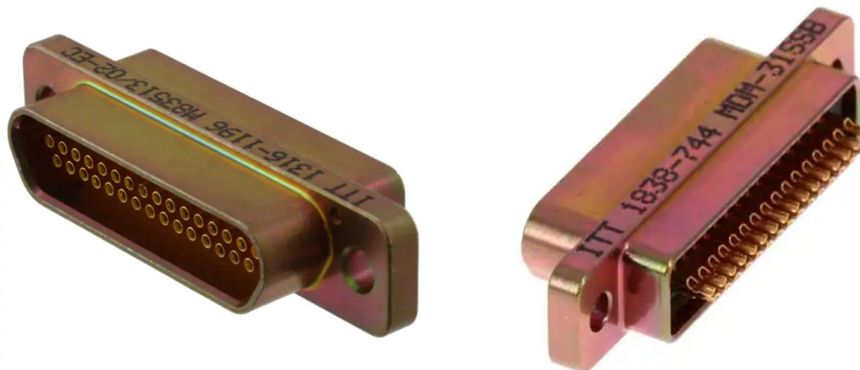


(a) (b)

Figure 4.3: Here **(a)** is a render of the Motherboard and **(b)** is the bottom of the cell that the Motherboard connects into.

An adapter (shown in Fig. 4.4) was needed to connect the pins from the Male Micro-D connector in the cell to the board. The solder-cup back of the adapter meant that there was some variability in the height we could choose between the board and the adapter.

The schematic for the board is presented in Fig. 4.6. The PCB design of the traces and the positioning of the various components are shown in Fig. 4.5.



(a) Front female sockets (b) Back solder cups

Figure 4.4: M83513/02-EC female Micro-D 31-socket adapter from ITT Cannon, LLC.

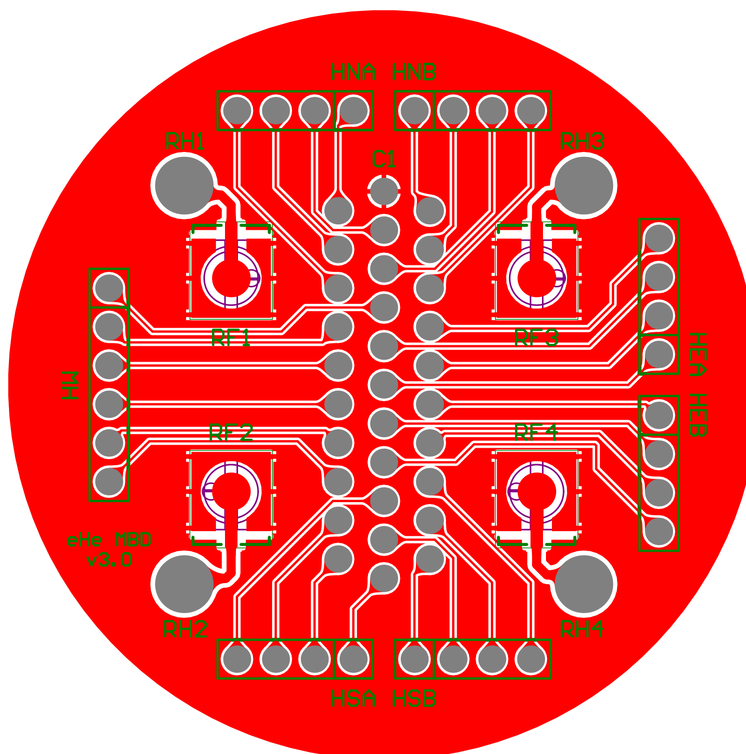


Figure 4.5: The PCB design and layout of the Motherboard. Red represents the top copper. The widths of the traces were a nominal 0.15 mm.

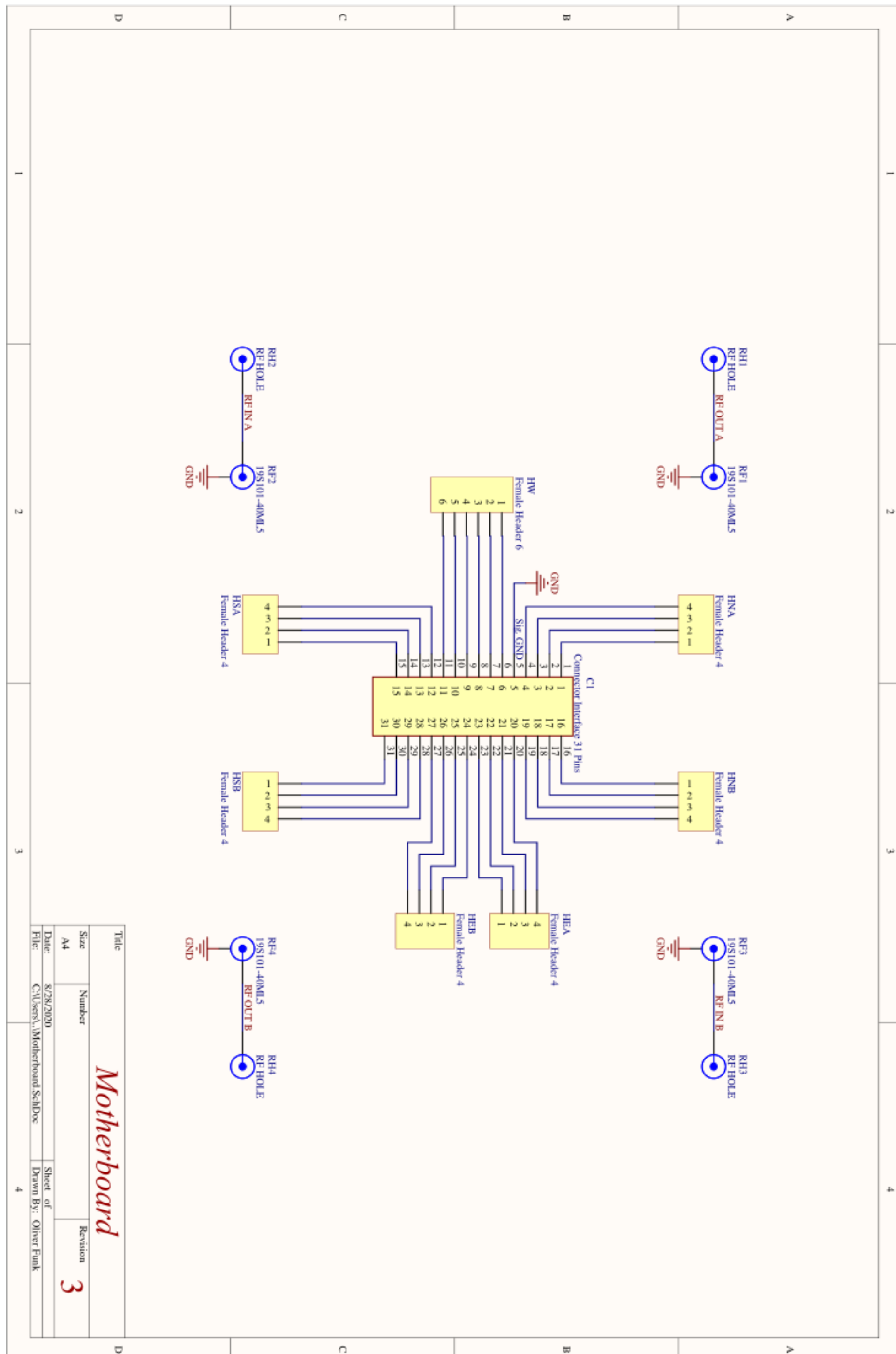


Figure 4.6: The schematic of the Motherboard.

4.3 Device Holding Board

The Device Holding Board was designed to hold and connect to the fabricated device, using wire bonds. These wire bonding pads can be seen around the central square area on the top of the board.

(a) Render Top

(b) Render Bottom

(c) PCB Top

(d) PCB Bottom

Figure 4.7: Here **(a)** and **(b)** show renders for the top and bottom of the Device Holding Board. **(c)** and **(d)** show the PCB designs for the top and bottom sides of the board.

The large central square pad in the top layer of the PCBs was needed to connect to the silicon substrate of the device and bias it. This is done by scratching its surface slightly and applying conductive silver paste to it. Generally, this would be grounded, but it is useful to have control over it during charge loading, as the device needs to be substantially more attractive to the electrons than the surrounding PCB and ground planes.

On the bottom side of the PCBs one can see the SMD RF interconnects

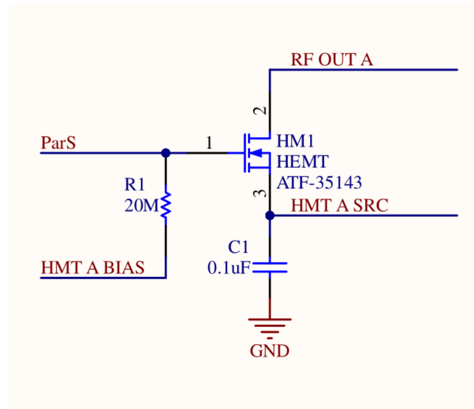


Figure 4.8: The schematic of the HEMT pre-amplifier. As can be seen, the sense gate signal (labelled ParS in this case) was connected directly to the HEMT's input gate and was biased through the resistor. The HEMT's drain was the output RF signal, connected to the coaxial lines, and while the source was biased to ground through a filtering capacitor.

and the HEMT pre-amplifier components (schematically shown in Fig.4.8). The positioning of the HEMT was critical as the length of the trace from any sense line to the HEMT's gate would increase the parasitic coupling to the ground plane. It was also very important that there was at least some grounded copper between any sense line and any twiddle line. Without it, any surface charge above the helium film above the PCB would be picked up as noise in the sensed signal.

Each sense line was connected to a pull-down resistor that itself had a controllable bias voltage applied to it. This allowed one to control the voltage around which the sense signal oscillated. The design of the amplifier also included a filtering capacitor in the source gate line that would pass higher frequency signals to GND.

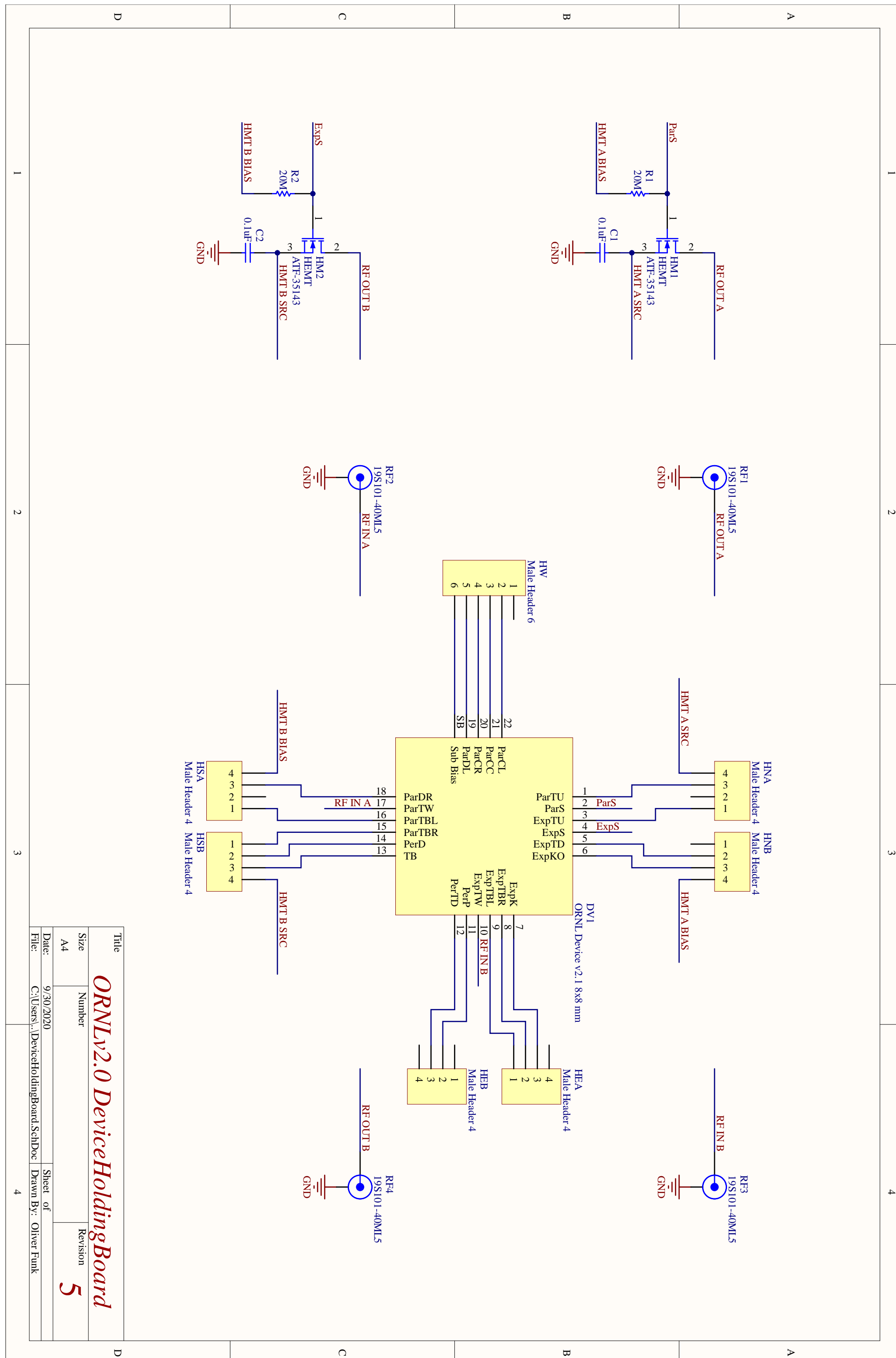


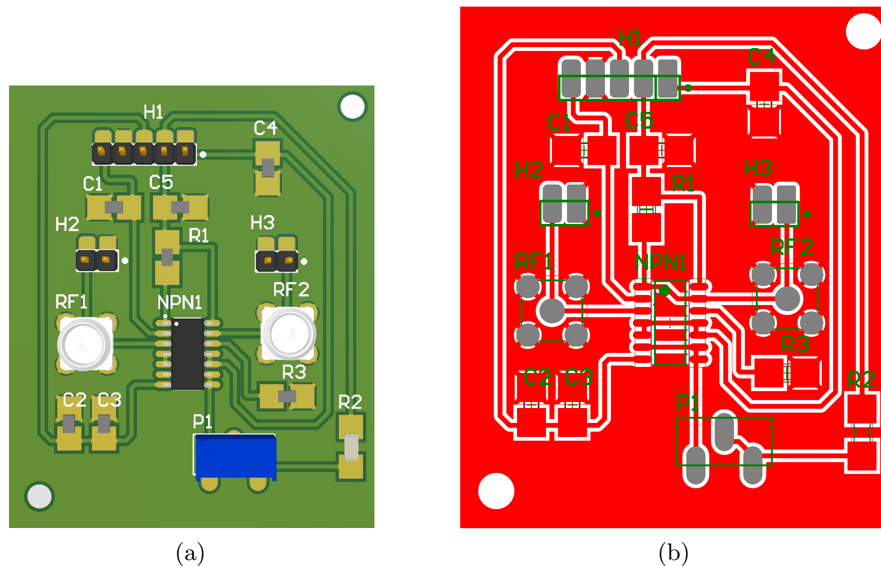
Figure 4.9: The schematic of the Motherboard.

4.4 Cascode Amplifier

An amplifier was needed to amplify the charge sensing signal coming from the HEMT pre-amplifier, detailed in the previous section. This amplifier was meant to be designed, built and tested as part of work done in this dissertation in 2020, however due to the various lockdowns put in place because of COVID-19, this could not be done as none of the required infrastructure was available (such as the tools needed to make the PCB, bench power supplies, oscilloscopes etc.).

Presented in this section is the design and testing of a Cascode amplifier given to this project by Dr Forrest Bradbury, which he had used as part of his PhD and had shown to work well. Initially, this was only meant to be a baseline amplifier implementation to test any subsequent designs against.

This Cascode amplifier used the MAT14ARZ IC, having four NPN BJTs in it with diodes connected between each gate and emitter. The amplifier consisted of two stages. The first stage, using BJT 1, was connected in a cascade configuration with the HEMT pre-amp. The second stage, using BJTs 2 and 3, were connected in a current mirror configuration, with the mirrored current being controllable using the Trim Pot and the other current coming from the HEMT's source gate. This was done to force it into an always ON state. Given the high input impedance of the HEMT and the fact that it was always on meant the entire configuration would be able to amplify small changes in voltages, at the cost of consuming more current.



(a) (b)

Figure 4.10: Here **(a)** shows a render of the Cascode amplifier and **(b)** shows the PCB design for the board.

The design of the Cascode PCBs (shown in Fig. 4.10) was done targeting the capabilities of the CNC routing machine available in the Physics department at UCT. The traces and gap sizes were had to be made larger than those of the previously detailed boards. This was possible given the relative simplicity of the design and the need for only a single side of metal.

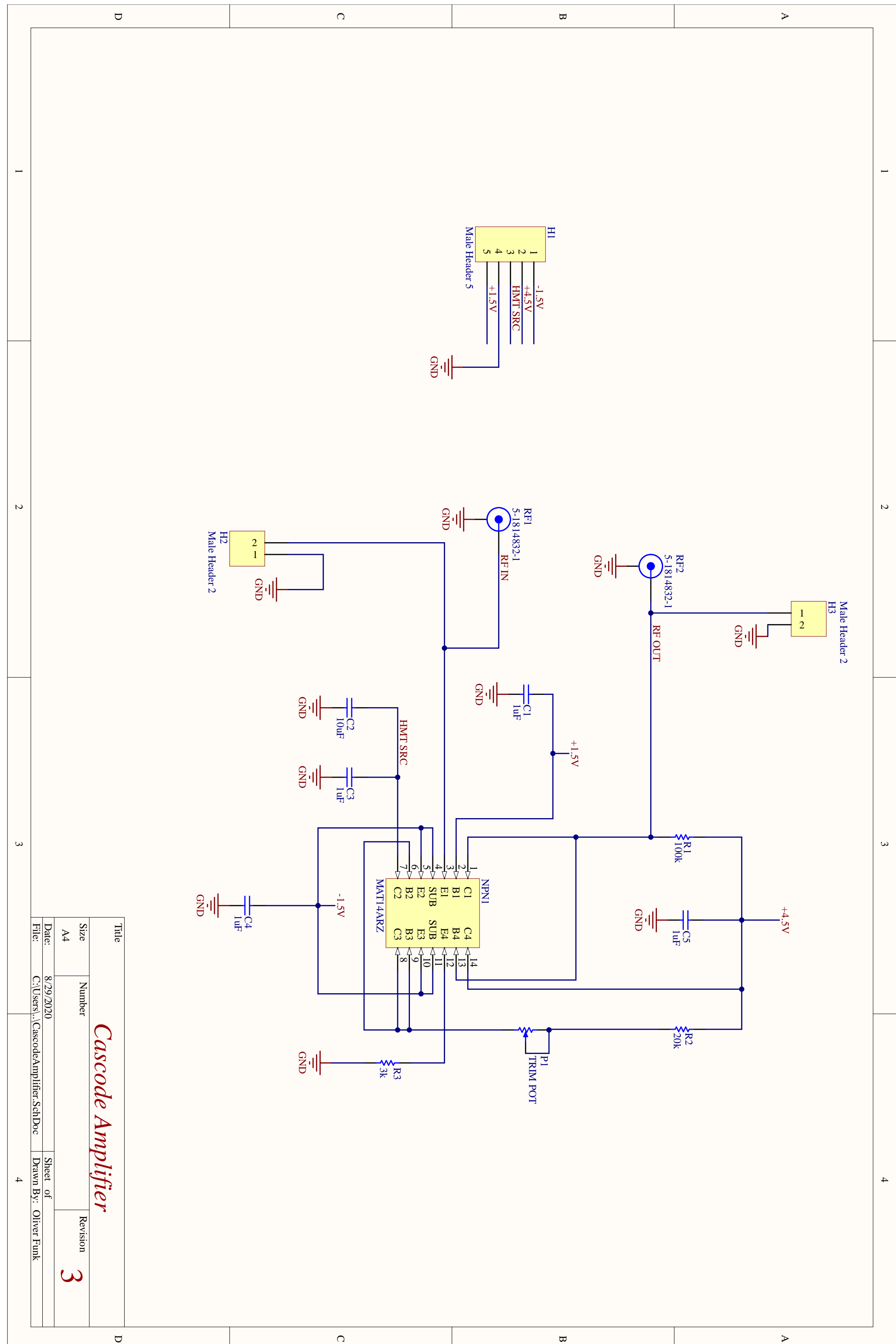


Figure 4.11: The schematic of the Cascode Amplifier.

4.4.1 Testing

The Cascode amplifier, along with pre-amplifier, were tested together to find the gain of the setup, as well as to determine if the pre-amplifier would work at low temperatures.

A test board had to be constructed for the HEMT pre-amplifier, shown in Fig. 4.12 **(a)**. This test board was submerged in liquid nitrogen in a polystyrene cup during the test as an approximation for the conditions inside the cell. A sinusoidal voltage at $f = 100\,\mathrm{kHz}$ was inputted across the R1 resistor and was biased around $50\,\mathrm{mV}$ to make sure the HEMT never turned off. A gain of $G = 22$ was recorded in the output, with a phase lag of approximately $3\pi/5$ radians (108 degrees).

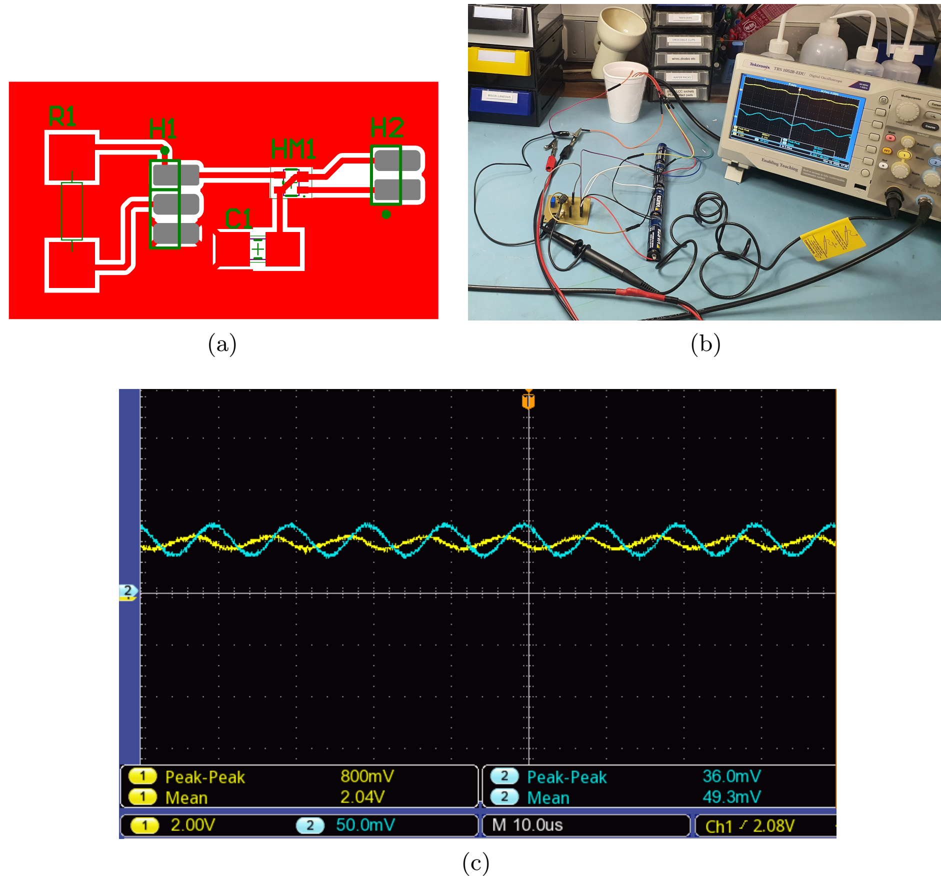


Figure 4.12: The PCB design for the HEMT pre-amplifier test board is shown in **(a)**, while the experimental setup to test the Cascode amplifier and HEMT is shown in **(b)**. The oscilloscope readings for the test is shown in **(c)**. The sinusoidal input signal ($f = 100\,\text{kHz}$) is in blue, with a vertical scale of $50\,\text{mV}$ per division, while the output in yellow, with a vertical scale of $2\,\text{V}$ per division. Both had the same time scale of $10\,\mu\text{s}$. The output signal is centred around $2\,\text{V}$, which was set by the bias voltages applied to the cascode amplifier. The amplification resulted in an phase lag of approximately $3\pi/5$ radians (108 degrees) in the output with a recorded gain of $G = 22$.

CHAPTER 5

HERMETIC CELL & DILUTION REFRIGERATOR PROBE

5.1 Hermetic Cell

The hermetically sealed superfluid cell was designed in collaboration with Dr Jay Amrit from Université Paris-Sud, France and is shown in Fig. 5.1.

A superfluid helium fill line can be seen coming into the cell from the top. Four coaxial RF cables run in from the top around the side of cell as well as a large cable around the side, which internally holds smaller individual cables for each biasing signal. The cell had to be superfluid leak-tight meaning each connector had to be hermetic and specially chosen. Another important consideration was good thermal anchoring of the cell to the probe that lowered it into the bottom of the dilution fridge (detailed in the next section). If the contact surface area between the two was not sufficiently large, it would take extremely long to cool the cell down.

A circular connector can also be seen coming out the top of the cell. This provided the additional pins needed for the tungsten filament for the thermal emission of electrons, as well as for miscellaneous components such as a depth measurement device to measure the bulk superfluid level.

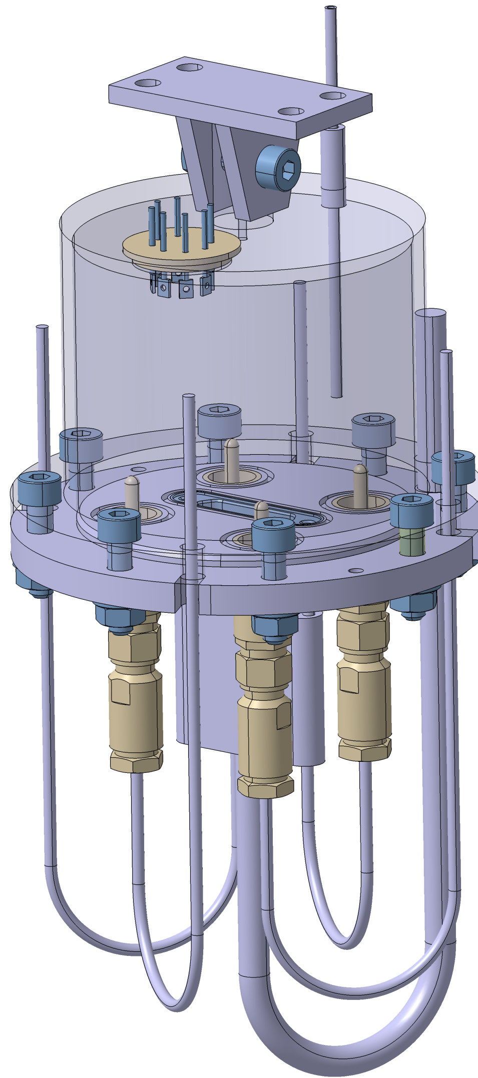
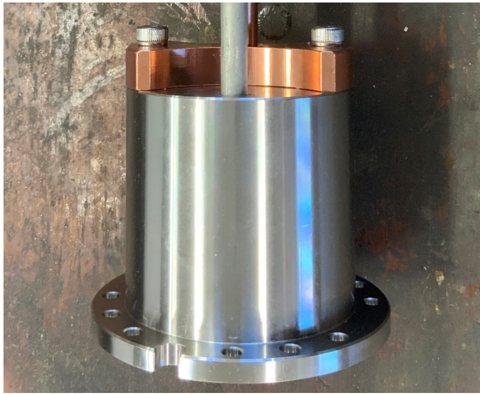


Figure 5.1: A render of the assembly of the hermetic cell. Image from Dr Jay Amrit, Université Paris-Sud.

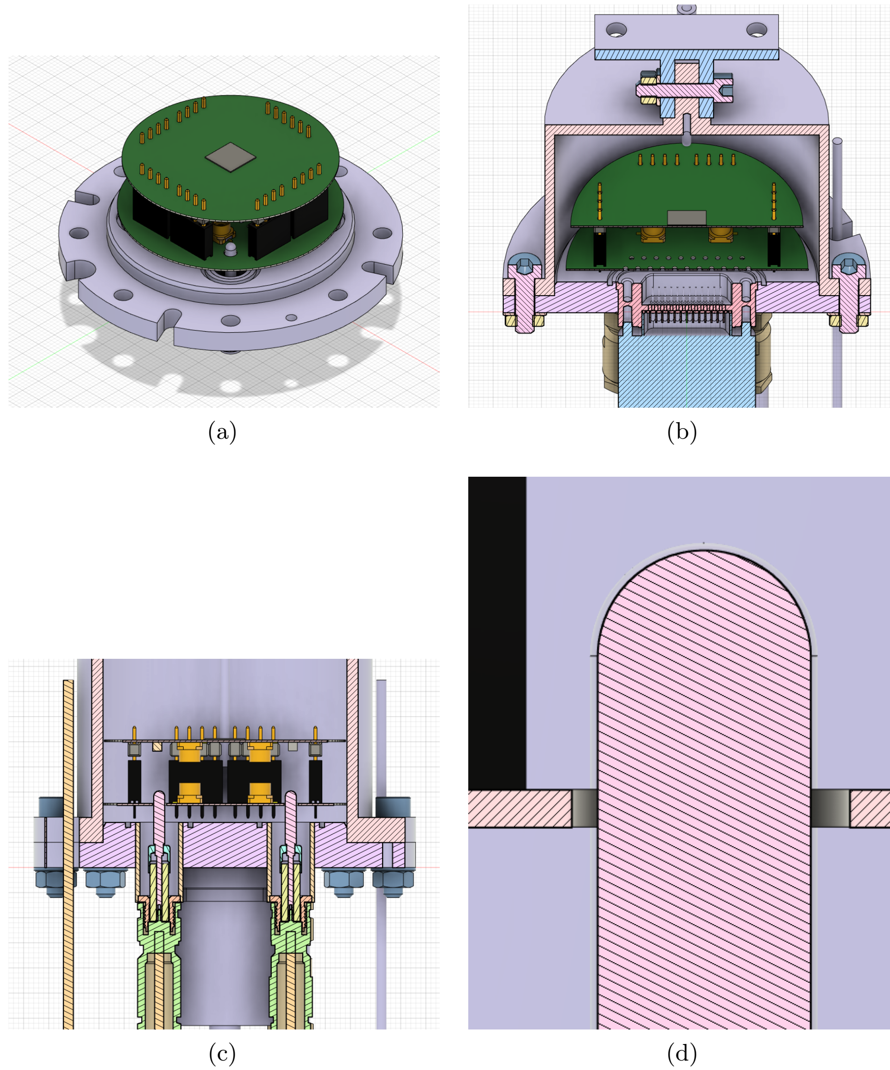


(a) The cell vacum chamber

(b) Inside of the vacum chamber

(c) The bottom flange with the DC connector attached.

Figure 5.2: The machined cell. The machining was done by the technicians in the UCT Physics workshop. The four RF feed-through connectors had not been soldered into the flange shown in figure **(c)** at the time the picture was taken.

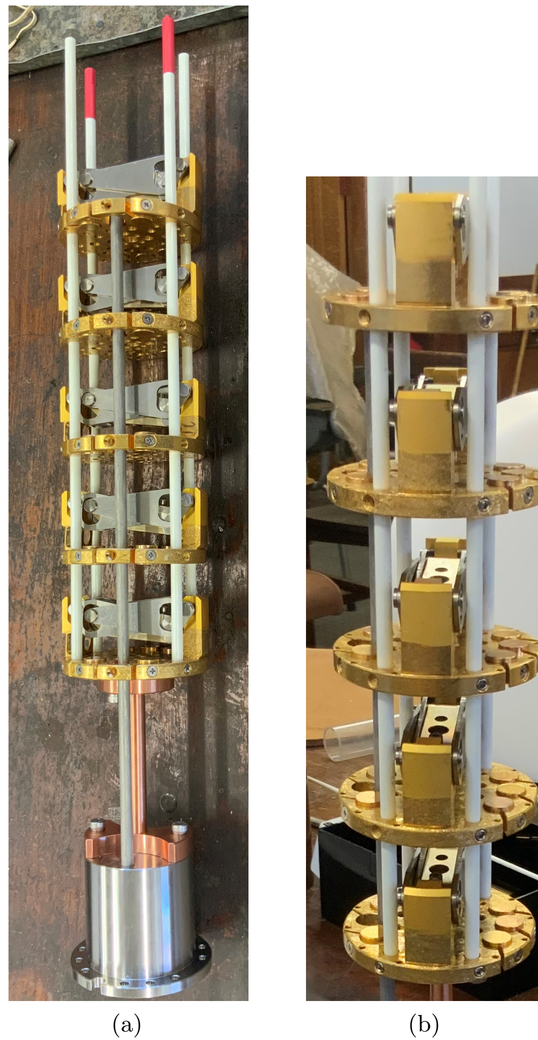


(a) (b) (c) (d)

Figure 5.3: Assembly of the PCBs inside the hermetic cell. The render in **(a)** shows the boards mounted onto the bottom of the cell, and in **(b)** a slice through the assembly showing how the boards fit into the cell and how the 31-pin connector in the cell aligns with the holes on the Motherboard. The render in **(c)** shows a slice through the assembly depicting the alignment of RF pins with the holes in the Motherboard, and in **(d)** a close-up of an RF pin and the mounting hole in the Motherboard.

5.2 Dilution Refrigerator Probe

The probe used to lower and dock the hermetic cell into the bottom of the dilution refrigerator is shown in Fig. 5.4. This probe had to be rebuilt for this project and fitted to the hermetic cell. The thermally-anchored copper connector can be seen at the bottom of the probe in Fig. 5.4 **(a)**. The probe has various clamps that align with and connect to each thermal plate inside the dilution chamber, shown in Fig. 5.5. It is important that proper physical contact is made between all components inside the chamber to cool them down.



(a) (b)

Figure 5.4: The probe used to lower the cell into the bottom of the dilution chamber. The temperature plate clamps can be seen in **(a)** with another view in **(b)**.

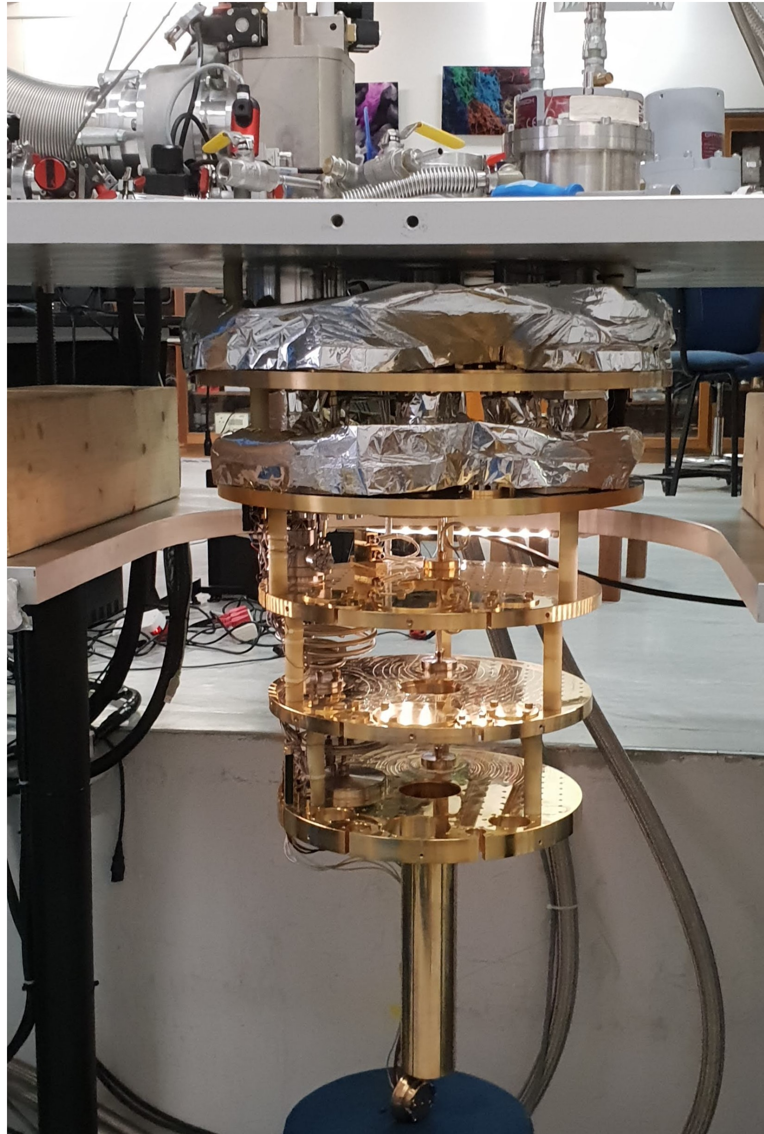


Figure 5.5: The inside of the dilution refrigerator in the UCT Physics NanoElectronics lab. One can see the various temperature plates with the central line of sight central port running through them. The probe is lowered through this opening and clamps solidly to each temperature plate to maintain a high level of thermal contact.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 Concluding Remarks

The results presented in this thesis have laid down the foundation needed to take this project further. Many of the components required by this project have either been completed or been brought close to completion.

Despite the progress made, due to the various lock-downs instituted globally because of the COVID-19 pandemic, it was not possible to conduct all planned experiments and a working device could not be successfully fabricated this year. Therefore, some of the answers to the research questions stated in the introduction could not be determined.

6.2 Device Design and Fabrication

Finalising the design of the device presented in Chapter 3 is one of the major contributions of this thesis. Months of iterative work and much back and forth between the relevant parties was needed to arrive at the final design. Multiple FEM analyses were performed on the device to determine the required fabrication tolerance parameters, as well as finding suitable voltage signals to apply the device's turnstile gates to achieve quantised single electron transport. The mathematical modelling that has been done is also very important as it gives a basis for the understanding of how the device works.

The device fabrication process (given in App. A) was also a major contribution of this thesis. Because the design was for a completely new kind of device that would push the achievable tolerances of the facilities at cleanroom used at CNMS at Oak Ridge Nation Labs, every fabrication step had to be determined from scratch, as there was very little to base it on. This meant many tests and experiments were needed to find what would work and what would not. A great deal of success was enjoyed in this regard, which was the result of a cumulative five weeks spent in the cleanroom (after two trips to the USA), as well as many informative meetings before and afterwards.

Further work is, however, needed to explore solutions to the alignment problems seen between the channels and the bottom gates and the tapering observed in the gap widths towards the top and bottom of the bottom electrodes (as detailed in Sec. 3.5). These are the last problems that need to be solved before a device can be successfully fabricated.

More tests are needed to resolve the observed alignment problem, as there were issues with the EBL during the time when the final device was fabricated, which may have been the cause.

The tapering issue may be solved by splitting the EBL step into two parts. First, the larger areas would be exposed and etched, followed by exposing and etching the much smaller gaps between the gates. The idea being that this would reduce the effect of secondary electrons overexposing the gap lines, causing the broadening. This would come at the cost of increasing the processing time and complexity, however.

Further collaboration with the team at CNMS is needed to come to a suitable path forward. A very important aspect of this thesis has been to establish a good relationship with CNMS. This will give future interested students from the NanoElectronics group the opportunity to visit the lab and get hands-on experience with nano-fabrication using the advanced equipment and facilities there.

Future students working on this project should be motived by the possibility of achieving the first result on the African continent of an electron on superfluid helium experiment, something worth pursuing.

6.3 Electronics, Integrating and Testing

The design of the electronics and PCBs, presented in Chapter 4, was another substantial contribution of this thesis.

Given the sensitive nature of the signals that are inputted and outputted from the device, many considerations had to be taken into account during the design of the PCBs. It was important to keep cross-talk between traces to a minimum, as well as reduce their length to keep the total line capacitance as low a possible. Custom SMD pads were included in the design, to allow

for some flexibility in choosing which parts of the device would be active (instead of using a different PCB each time). Additionally, custom footprints were needed to integrate with the various connector interfaces present inside the hermetic cell.

The hermetic cell and dilution fridge probe, presented in Chapter 5, were successfully machined and assembled as part of this thesis. These form the last of the core infrastructural requirements needed by this project.

Further work is needed to test the integration of the PCBs with the cell and the probe and to install it all into the dilution fridge. The cell would need to be successfully filled with superfluid helium and checked for leaks, by measuring the fluid level and making sure it remains constant. The electronics would then need to be tested, to ensure its successful operation at the required cryogenic temperatures.

6.4 Other Interesting Experiments

With changes to the design of the device, other interesting experiments can be conducted in this superfluid system.

Some possibilities include investigating the surface structure of superfluid ^{4}He as demonstrated by Kono et al. [7]. The curvature of the superfluid film could be measured as it bows down a channel, by measuring the charging effect of electrons as they move down it. Nano-rods could be fabricated into a channel to localise single electrons above it.

Experiments that require high coherence times could be conducted, such as those needed to investigated Aharonov–Bohm oscillations [18] or possibly in application to a quantum computing device, as detailed by Lyon [10].

These are all experiments worthwhile pursing, which would be made possible by the successful implementation of this interesting physical system, the only one on the African continent.

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APPENDIX A

FABRICATION PROCESS GUIDE

Layer:	L1 - BottomMetalPlate
Description:	This is a liftoff layer that defines the wafer alignment marks, wafer layout markers and the bottom metal for the bottom electrodes. **+ve photolith., metal deposition [5 nm Cr, 20 nm Au, 3 nm Cr]**
Plan	
Pre-process:	Use one of the prepared 3.5 um thermal oxide layer wafers. Spin rinse it before starting.
Spin resist:	The following is done in the EBL room: 1. Spin **P20** 2. Spin **LOR 3A** 3. Bake at **180C** for **2 minutes** Take the wafer to the photolith. room: 4. Spin **SPR 995-0.7** 5. Bake at **90C** for **90 seconds** (*All spin speeds are 3k RPM)
Pattern:	The following is done on the SUSS Mask Aligner: 1. Select recipe, save, exit - Recipe: **First.Mask** - Contact mode: **Vacuum Contact** (preferable, hard is also fine if you can't get vacuum) - Dose: **45 mJ/cm^3** 2. Put the mask in, chrome side up. The numbers by the alignment marks must be **away** from the MF side. 3. Load the wafer, make sure the stage's rotational alignment mark is lined up properly 4. Expose 5. 90 second post-exposure bake at 90C
Develop:	1. Ready a container of CD-26, remember to label and set a timer for 1 minute 2. Immerse and start the timer, while gently swirling the container around 3. Rinse with DI water and carefully dry with N2 4. Place wafer in the Tepla, in the faraday cage on the quartz boat - Recipe: **1-min Descum**
Process:	The following is done with the E-Beam evaporator: 1. Load wafer facing down into the wafer holder (align the MF to the thin edge side of the holder hole, otherwise it doesn't fit in properly). 2. Load the holder and start pumping down. Don't forget to do the checks and put a note on the door.

	3. Do the deposition, in order: a. **Cr - 5 nm** b. **Au - 20 nm** c. **Cr - 3 nm** 4. Vent after metal stops glowing, make sure the N2 is on.
Strip resist:	1. Ready three containers, **Acetone, IPA and CD-26**. Remember to label them. 2. Immerse wafer in Acetone and leave for around **30 minutes** 3. Sonicate a few times for **10 seconds** and leave to soak for another **30 minutes** 4. Take the wafer out of the Acetone container and flow with Acetone bottle to remove leftover flakes. 5. Immediately immerse in the IPA bath, do not let the Acetone evaporate! Gently move it around before immersing the wafer in the CD-26 bath. 6. Leave for 2 minutes, while gently swirl it around. 7. Take the wafer out and rinse with DI water followed by N2 dry. Use the spin rinser if you feel you need to. 8. O2 Plasma clean by placing the wafer in the RIE metal etcher - Recipe: **OPT - Chamber clean** - Time: **30 seconds** 9. Inspect under the microscope. If there is still resist left, redo chamber clean.

<table>
<tr><td>Layer:</td><td>L2 - BottomGates</td></tr>
<tr><td>Description:</td><td>This is an etch layer that defines the bottom metal electrodes using EBL.

+ve EBL, sputter etch through 28 nm of metal</td></tr>
<tr><td colspan="2">Plan</td></tr>
<tr><td>Pre-process:</td><td>None.</td></tr>
<tr><td>Spin resist:</td><td>The following is done in the EBL room:
1. Spin ZEP 520A
2. Bake at 180C for 3 minutes

(*All spin speeds are 3k RPM)</td></tr>
<tr><td>Pattern:</td><td>1. Load wafer into the EBL
2. Load files
3. Compile magazine file
4. Calibrate, find alignment marks and execute mag file</td></tr>
<tr><td>Develop:</td><td>1. Put the face shield on
2. Ready two containers, Xylenes and IPA. Don’t forget to label!
3. Ready the stopwatch for 40 seconds
4. Immerse wafer in the Xylenes and start the stopwatch
5. When the timer is up, take the wafer out and immerse in the IPA bath
6. Descumming isn’t necessary for this layer as it is an etch mask.</td></tr>
<tr><td>Process:</td><td>The following is done using the RIE Metal Etcher
1. Run a 10 minutes chamber clean (unless it was done beforehand).
2. Load the wafer and start the process
- Recipe: OPT - Sputter Etch
- Time: 30 seconds
3. Check that the etch went through under the microscope
4. Do it for a bit longer if it did not.</td></tr>
<tr><td>Strip resist:</td><td>1. Place the wafer in the wafer holder, on the NMP bench
2. Place the wafer holder into the hot NMP bath. Make sure the heat is ON!
3. Leave for around 1 hour
4. Prepare a container of NMP and heat it up. Don’t forget the label!
5. Once warm, place the wafer in it and sonicate for 10 seconds
6. Place the container with the wafer in it, back into the NMP bath. Leave for 10 minutes.
7. Take the wafer out, rinse gently with DI water and dry with N2 Use the spin rinser if you want to.
8. O2 Plasma clean by placing the wafer in the RIE metal etcher</td></tr>
</table>

	- Recipe: **OPT - Chamber clean** - Time: **30 seconds** 9. Inspect under the microscope. If there is still resist left, redo chamber clean.

Layer:	L3 - BottomPads
Description:	This is a liftoff layer that defines the bottom traces and bonds pads. **+ve photolith., metal deposition [10 nm Cr, 50 nm Au, 10 nm Cr]**
Plan	
Pre-process:	None.
Spin resist:	The following is done in the EBL room: 1. Spin **P20** 2. Spin **LOR 3A** 3. Bake at **180C** for **2 minutes** Take the wafer to the photolith. room: 4. Spin **SPR 995-0.7** 5. Bake at **90C** for **90 seconds** (*All spin speeds are 3k RPM)
Pattern:	The following is done on the SUSS Mask Aligner: 1. Select recipe, save, exit - Recipe: **TSA.AL** - Contact mode: **Hard Contact** - Dose: **45 mJ/cm^3** 2. Put the mask in, chrome side up. The numbers by the alignment marks must be **on** the MF side. 3. Find the alignment marks - Offset: **+/- 40 000** 4. Load the wafer, make sure the stage's rotational alignment mark is lined up properly 5. Align the wafer to the mask 6. Expose 7. 90 second post-exposure bake at 90C
Develop:	1. Ready a container of CD-26, remember to label and set a timer for 1 minute 2. Immerse and start the timer, while gently swirling the container around 3. Rinse with DI water and carefully dry with N2 4. Place wafer in the Tepla, in the faraday cage on the quartz boat - Recipe: **1-min Descum**
Process:	The following is done with the E-Beam evaporator: 1. Load wafer facing down into the wafer holder (align the MF to the thin edge side of the holder hole, otherwise it doesn't fit in properly). 2. Load the holder and start pumping down. Don't forget to do the checks and put a note on the door. 3. Do the deposition, in order:

	a. **Cr - 10 nm** b. **Au - 50 nm** c. **Cr - 10 nm** 4. Vent after metal stops glowing, make sure the N2 is on.
Strip resist:	1. Ready three containers, **Acetone, IPA and CD-26**. Remember to label them. 2. Immerse wafer in Acetone and leave for around **30 minutes** 3. Sonicate a few times for **10 seconds** and leave to soak for another **30 minutes** 4. Take the wafer out of the Acetone container and flow with Acetone bottle to remove leftover flakes. 5. Immediately immerse in the IPA bath, do not let the Acetone evaporate! Gently move it around before immersing the wafer in the CD-26 bath. 6. Leave for 2 minutes, while gently swirl it around. 7. Take the wafer out and rinse with DI water followed by N2 dry. Use the spin rinser if you feel you need to. 8. O2 Plasma clean by placing the wafer in the RIE metal etcher - Recipe: **OPT - Chamber clean** - Time: **30 seconds** 9. Inspect under the microscope. If there is still resist left, redo chamber clean.

<table>
<tr><td>Layer:</td><td>L4 - TopPlates</td></tr>
<tr><td>Description:</td><td>This is an oxide deposition and liftoff layer that defines the height of the channels and puts down the top metal layer

Oxide deposition [20 nm ALD Al2O3, 30 nm ALD SiO2, 650 nm PECVD SiO2, 50 nm ALD SiO2]
+ve photolith., metal deposition [5 nm Cr, 10 nm Au]</td></tr>
<tr><td colspan="2">Plan</td></tr>
<tr><td>Pre-process:</td><td>1. Load the wafer into the ALD machine
2. Start the process (should take around 30 minutes to complete):
- Recipe: OPT - Al2O3 @ 150
- Cycles: 150 cycles [20 nm]
3. Start a new process on the same wafer (should take around 56 minutes to complete):
- Recipe: OPT - SiO2 @ 150
- Cycles: 250 cycles [30 nm]
4. Load the wafer into the PECVD machine, make sure you have run a 5 minute pre-condition run on the dummy wafer before
5. Start the process (remember to run the a chamber clean after):
- Recipe: OPT - SiO2 - Low Rate
- Time: 10:00 [650 nm]
6. Load the wafer into the ALD machine
7. Start the process (should take around 1 hour 30 minutes to complete):
- Recipe: OPT - SiO2 @ 150
- Cycles: 417 cycles [50 nm]</td></tr>
<tr><td>Spin resist:</td><td>The following is done in the EBL room:
1. Spin P20
2. Spin LOR 3A
3. Bake at 180C for 2 minutes

Take the wafer to the photolith. room:
4. Spin SPR 995-0.7
5. Bake at 90C for 90 seconds

(*All spin speeds are 3k RPM)</td></tr>
<tr><td>Pattern:</td><td>1. The following is done on the SUSS Mask Aligner:
2. Select recipe, save, exit
- Recipe: TSA.AL
- Contact mode: Soft Contact
- Dose: 45 mJ/cm^3
3. Put the mask in, chrome side up. The numbers by the alignment marks must be on the MF side.
4. Find the alignment marks
- Offset: +/- 41 000
5. Load the wafer, make sure the stage’s rotational alignment mark</td></tr>
</table>

	is lined up properly 6. Align the wafer to the mask 7. Expose 8. 90 second post-exposure bake at 90C
Develop:	1. Ready a container of CD-26, remember to label and set a timer for 1 minute 2. Immerse and start the timer, while gently swirling the container around 3. Rinse with DI water and carefully dry with N2 4. Place wafer in the Tepla, in the faraday cage on the quartz boat - Recipe: **1-min Descum**
Process:	The following is done with the E-Beam evaporator: 1. Load wafer facing down into the wafer holder (align the MF to the thin edge side of the holder hole, otherwise it doesn't fit in properly). 2. Load the holder and start pumping down. Don't forget to do the checks and put a note on the door. 3. Do the deposition, in order: **a. Cr - 5 nm** **b. Au - 10 nm** 4. Vent after metal stops glowing, make sure the N2 is on.
Strip resist:	1. Ready three containers, **Acetone, IPA and CD-26**. Remember to label them. 2. Immerse wafer in Acetone and leave for around **30 minutes** 3. Sonicate a few times for **10 seconds** and leave to soak for another **30 minutes** 4. Take the wafer out of the Acetone container and flow with Acetone bottle to remove leftover flakes. 5. Immediately immerse in the IPA bath, do not let the Acetone evaporate! Gently move it around before immersing the wafer in the CD-26 bath. 6. Leave for 2 minutes, while gently swirl it around. 7. Take the wafer out and rinse with DI water followed by N2 dry. Use the spin rinser if you feel you need to. 8. O2 Plasma clean by placing the wafer in the RIE metal etcher - Recipe: **OPT - Chamber clean** - Time: **30 seconds** 9. Inspect under the microscope. If there is still resist left, redo chamber clean.

Layer:	L5 - TopThickenning
Description:	This is a liftoff layer that thickens top metal bond pads **+ve photolith., metal deposition [50 nm Au]**
Plan	
Pre-process:	None.
Spin resist:	Doing the following in the photolith. room (LOR isn't necessary for this layer): 1. Spin P20 2. Spin SPR 995-0.7 3. Bake at 90C for 90 seconds (*All spin speeds are 3k RPM)
Pattern:	The following is done on the SUSS Mask Aligner: 1. Select recipe, save, exit - Recipe: **TSA.AL** - Contact mode: **Soft Contact** - Dose: **45 mJ/cm^3** 2. Put the mask in, chrome side up. The numbers by the alignment marks must be **on** the MF side. 3. Find the alignment marks - Offset: **+/- 42 000** 4. Load the wafer, make sure the stage's rotational alignment mark is lined up properly 5. Align the wafer to the mask 6. Expose 7. 90 second post-exposure bake at 90C
Develop:	1. Ready a container of CD-26, remember to label and set a timer for 1 minute 2. Immerse and start the timer, while gently swirling the container around 3. Rinse with DI water and carefully dry with N2 4. Place wafer in the Tepla, in the faraday cage on the quartz boat - Recipe: **1-min Descum**
Process:	The following is done with the E-Beam evaporator: 1. Load wafer facing down into the wafer holder (align the MF to the thin edge side of the holder hole, otherwise it doesn't fit in properly). 2. Load the holder and start pumping down. Don't forget to do the checks and put a note on the door. 3. Do the deposition, in order: **a. Au - 50 nm** 4. Vent after metal stops glowing, make sure the N2 is on.
Strip resist:	1. Ready a container with Acetone

	2. Place wafer in the container and leave for 1 hour 3. Sonicate it for 10 seconds 4. Take the wafer out and flow with IPA. Do not let the Acetone dry! 5. Rinse with DI water and N2 dry. Use the spin rinser if you feel you need to. 6. O2 Plasma clean by placing the wafer in the RIE metal etcher - Recipe: **OPT - Chamber clean** - Time: **30 seconds** 7. Inspect under the microscope. If there is still resist left, redo chamber clean.

Layer:	L6 - Channels
Description:	This is an etch layer that defines the channels and exposes the bottom bondpads. The alignment of this layer to the bottom gates is critical. **+ve photolith., sputter etch, RIE etch, BHF 50:1 etch**
Plan	
Pre-process:	None.
Spin resist:	Doing the following in the photolith. room: 1. Spin **P20** 2. Spin **S1818** 3. Bake at **120C** for **2 minutes 30 seconds** (*All spin speeds are 3k RPM)

Pattern:	The following is done on the SUSS Mask Aligner:
	1. Select recipe, save, exit
	    - Recipe: **TSA.AL**
	    - Contact mode: **Vacuum Contact**
	    - Dose: **65 mJ/cm^3**
	2. Put the mask in, chrome side up. The numbers by the alignment marks must be **on** the MF side.
	3. Find the alignment marks
	    - Offset: **+/- 43 000**
	4. Load the wafer, make sure the stage's rotational alignment mark is lined up properly
	5. Align the wafer to the mask
	6. Expose
	7. Do a 60 second post-exposure bake at 120C

Develop:	1. Ready a container of CD-26, remember to label and set a timer for 1 minute 2. Immerse and start the timer, while gently swirling the container around 3. Rinse with DI water and carefully dry with N2 4. Descumming **isn't** necessary for this layer as it is an etch mask.

Process:	1. Load the wafer into the RIE Metal Etcher (make sure a chamber clean was done before, at least 10 minutes long).
	2. Run process
	    - Recipe: **OPT - Sputter Etch**
	    - Time: **20 seconds**
	3. Run another process on the same wafer
	    - Recipe: **OPT - SiO2 (OLD)**
	    - Time: **2:30 seconds**
	
	Do the following at the White Bench:

	4. Place the wafer container on the white bench with the lid unscrewed 5. Wear the necessary PPE and prepare two containers, one with BHF 50:1 and the other with DI water. Remember to label. 6. Prepare a timer for **60 seconds** 7. Start the timer after immersing the wafer into BHF solution (be careful, the wafer **hydrophobically floats** on top of the BHF) 8. Once the timer finishes, immediately place the wafer into the container of **DI water**

Strip resist:	1. Place the wafer in the wafer holder, on the NMP bench
	2. Place the wafer holder into the hot **NMP bath**. Make sure the heat is ON!
	3. Leave for around **1 hour**
	4. Take the wafer out, rinse gently with DI water and dry with N2 Use the spin rinser if you want to.
	5. O2 Plasma clean by placing the wafer in the RIE metal etcher
	    - Recipe: **OPT - Chamber clean**
	    - Time: **15 seconds**
	6. Inspect under the microscope. If there is still resist left, redo chamber clean.